A CAHNERS PUBLICATION
INTERNATIONAL EDITION
NOVEMBER 24, 1988

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Analog-simulation packages increase your chances of meeting design specs

SIEMENS

Optocouplers for mains separation

Certified for a secure future

People need to be protected from electric shocks, is what the law says. Just like electronics need to be protected from voltage spikes, as the designer says.

Optocouplers do both. They are designed to give safe electrical isolation.

Coupling without risk = secure mains isolation, secure data transmission, secure (longterm) function and assured certification of your electronic devices.

Electric shocks – hazardous to people – don't have to trouble you any more. Put in a mains isolator from Siemens. And as an extra benefit, you can forget those processor-killing voltage spikes.

Siemens mains isolators are approved and certified. Millions of units have withstood the VDE 0883 test spec, and they are now also available individually measured to the VDE 0884 spec, each unit being tested for freedom from partial discharge (option 1), or you can have them with controlled burn-in (option 2).

For more details, just write Siemens AG, Infoservice B-Z568, Postfach 23 48, D-8510 Fürth, West Germany, quoting "Mains isolators".

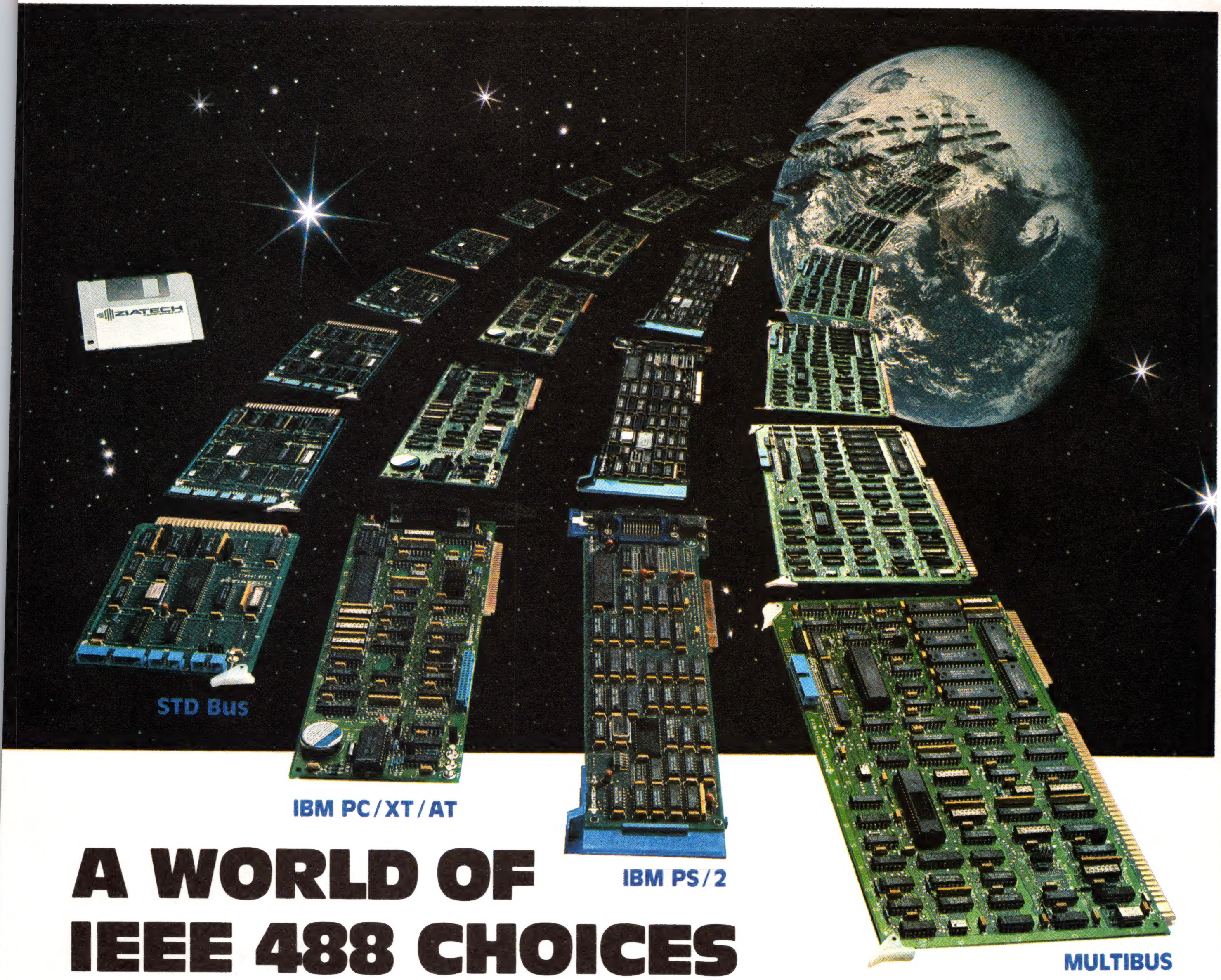
TopTech Components – Siemens

CIRCLE NO 125

A 19100-B-Z568-X-7600

electronica '88
Munich

8.–12.11.88
Siemens, Hall 23, Position A 4

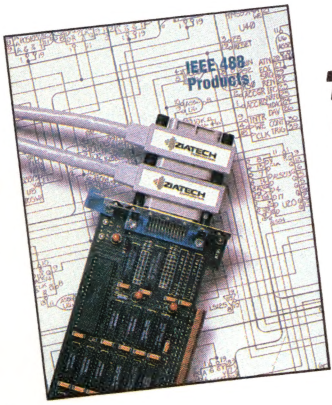


A WORLD OF IEEE 488 CHOICES

For OEM applications

Hardware interfaces and software drivers for OEMs who depend on superior products, pricing and technical support to make their products succeed.

Hardware interfaces for the IBM PS/2, PC/XT/ATs, STD Bus and MULTIBUS systems.



The WORD on IEEE 488 choices

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Software Choices

Several software driver choices for each interface. Also, the menu-driven ASYSTANT GPIB package for scientific instrument control and data analysis.

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Ziatech's world also includes STD Bus computers, software development systems, and local industrial networks for test and control applications.

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CIRCLE NO 111

WHY VTC? ASK THE VME CONSORTIUM.

"For a bunch of companies that don't always agree on everything, we sure were unanimous on VTC."

The VME Consortium needed an economical, yet highly functional VME bus interface chip, to minimize design time . . . and to help raise the VME standard to higher levels.

"We looked at the leading suppliers," said Joe Ramunni, consortium chairman (and president of Mizar), "and VTC came out on top. Their CMOS standard-cell ASIC approach gave us the high drive capability we needed, optimized for bus interfacing. And, it proved much more cost-effective, with higher performance, than gate array technology."

The VME Consortium is made up of such firms as Plessey Microsystems, Omnibyte Corporation, Mizar Inc., Ironics Inc., Heurikon Corporation, Matrix Corporation, and Clearpoint Inc., among others. What did they look for in a supplier?

"We needed a credible business partner," said Ramunni, "with a proven track record, who could provide a turnkey package . . . both design and fab. A supplier that could produce in quantity, and provide technical support to the market at large.

"We also needed a firm with an international marketing structure, because we expect this chip to be the de facto standard worldwide.

"But, we needed *people* we could work with, too. VTC had the right 'comfort factor'."

Jack Regula, consortium technical director (and VP-R&D, Ironics) added: "Our requirements for high speed, high gate-count, low power consumption, and VME bus drive capability were all met well with VTC's 1-micron CMOS standard cell library. And we were extremely impressed with VTC's facilities, its people, and its customer list."

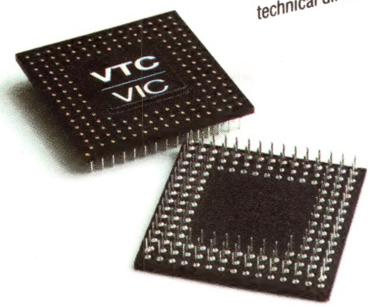
In the future, the VME bus chip (VIC) will become a standard cell within VTC's CMOS library, to allow customers to further customize the chip.

Shouldn't you be getting to know VTC, too? You'll be in good company when you do. Call or write us today, and we'll send you our short-form product catalog, which describes our product offerings in linear signal processing, high-speed CMOS logic, mass storage ICs, bipolar ASIC, and CMOS ASIC.

VTC Incorporated, 2401 East 86th Street, Bloomington, MN 55420. (In Minnesota, 612/851-5200.) Telex 857113.

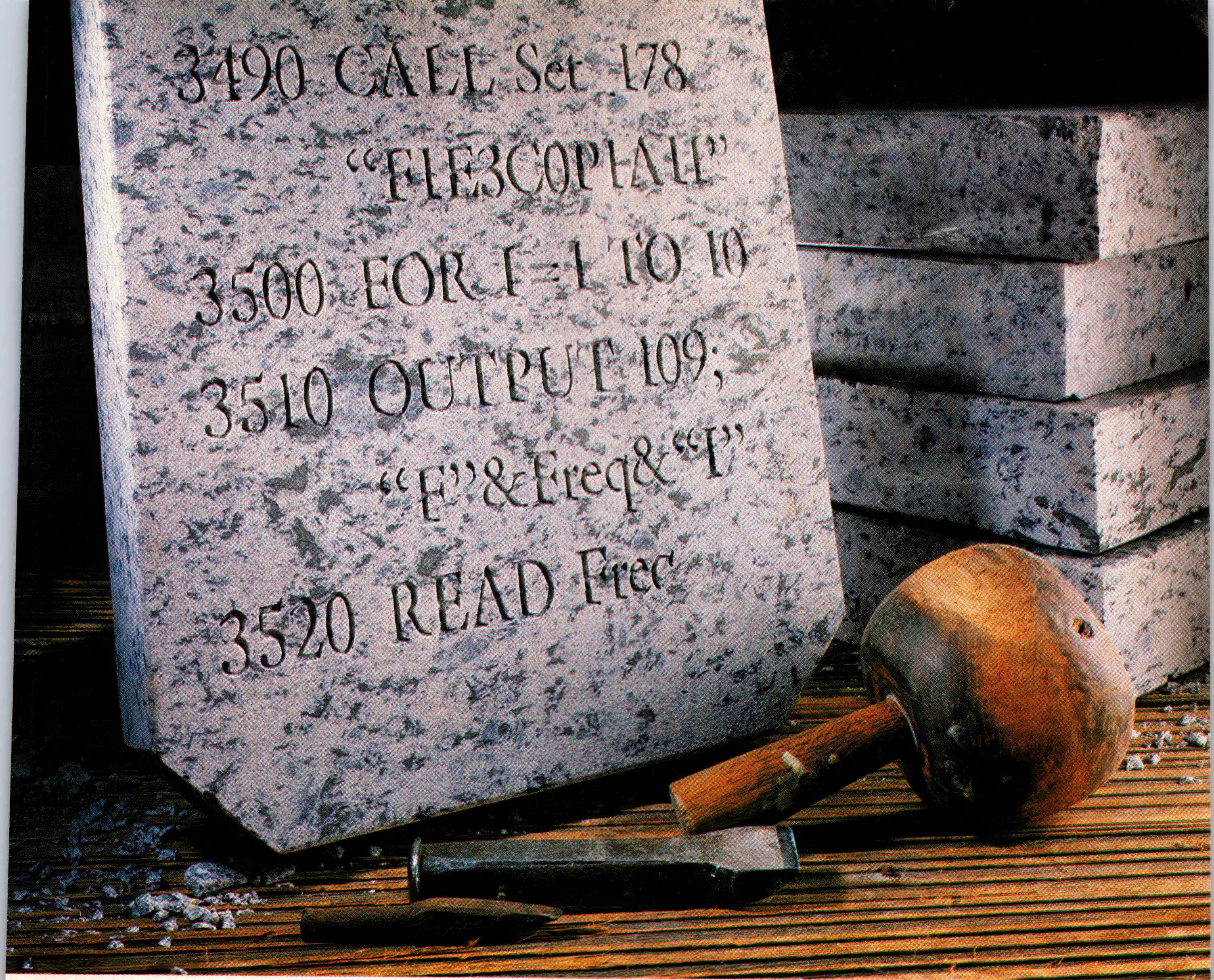
CALL 1-800-VTC-VLSI

Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.

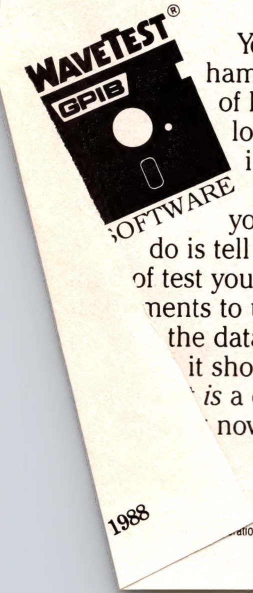


VTC Incorporated
Performance, Pure & Simple™

CIRCLE NO 110



Writing a GPIB program shouldn't take an eternity.



You shouldn't have to hammer out hundreds of lines of BASIC, or look up all those instrument commands. All you should have to do is tell the computer what of test you want to run, what nents to use, and what to the data.
it should do the rest.
is a computer.
now, that's how it'll be, if you have our new WaveTest® software.

Just point to the program elements you need, assemble them either as a flowchart or a string of icons. WaveTest writes all the program code, including the GPIB commands for more than fifty different makes and models of instruments.

You'll be able to take months off of test development. Best of all, you'll be putting your time into the design of the program—and not into tedious code writing. WaveTest runs on your PC-compatible computer and it uses Microsoft® Windows and a mouse, making it very user-friendly.

To write another program without WaveTest would be a basic error. For immediate information, call our Applications Department at (619) 279-2200.

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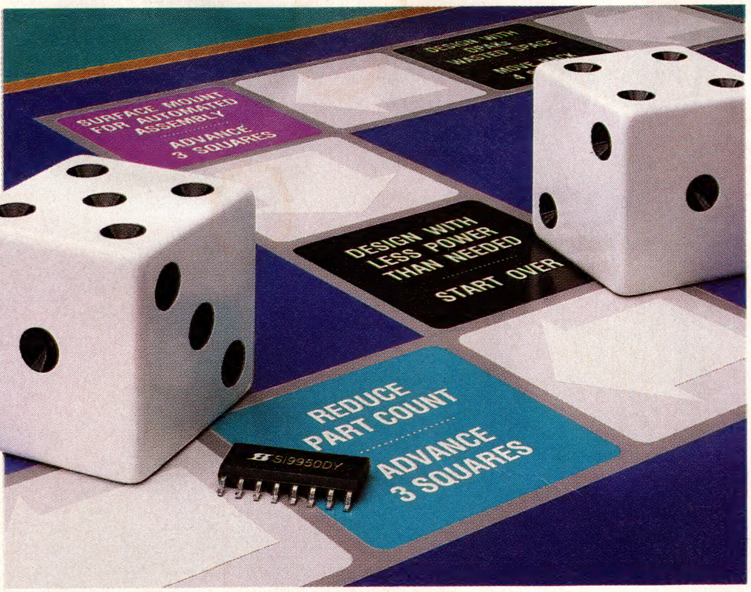
CIRCLE NO 70

WAVETEK

The smallest big move in motor control.



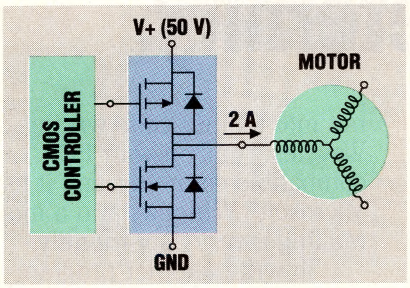
Siliconix' new surface mount MOSPOWER Half Bridge Driver delivers a powerful 2 A while occupying less space than DIPs & DPAKs.

Siliconix has just made a very big move—in a very small way. Now it's your turn!

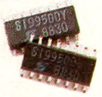
Save space! Improve reliability! Use your new half bridge driver in a tiny SO-16 surface mount package to replace two bulky MOSFETs in your motor control circuits.

And now that the through-hole devices are eliminated your assembly can be totally automated, reducing manufacturing cost and complexity.

The Si9950 contains 50 V complementary n- and p-channel MOSFETs that deliver the 2 amps you need for high performance. And the $r_{DS(ON)}$ of each transistor is only 0.3 Ω. Resulting in low, low power consumption with direct drive from CMOS control circuitry.



The Si9950 MOSPOWER driver is the perfect way to get more power into less space in motor control applications for disk drives, printers, copiers, plotters & battery-powered systems. It also makes an ideal MOSFET driver in high frequency power supplies.



Make your big move to Siliconix' small Si9950 MOSPOWER half bridge driver. Dial our toll-free hot line now! Call 1 (800) 554-5565, Ext. 942 for your free MOSPOWER Half Bridge Driver Design Kit. It includes your sample, data sheet and application note.

Siliconix
incorporated

2201 Laurelwood Road, Santa Clara, CA 95054

Volume 33, Number 24

EDN Magazine Edition

November 24, 1988

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: *Once you decide to try analog simulation, you'll have to figure out when to simulate during a project, and then weigh the tradeoffs between breadboarding and simulation. See pg 106. (Photo courtesy Analogy)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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BPA ABP

Continued from page 5

EDN Magazine Edition

November 24, 1988

The RISC design philosophy shows no signs of diminishing in popularity (pg 122).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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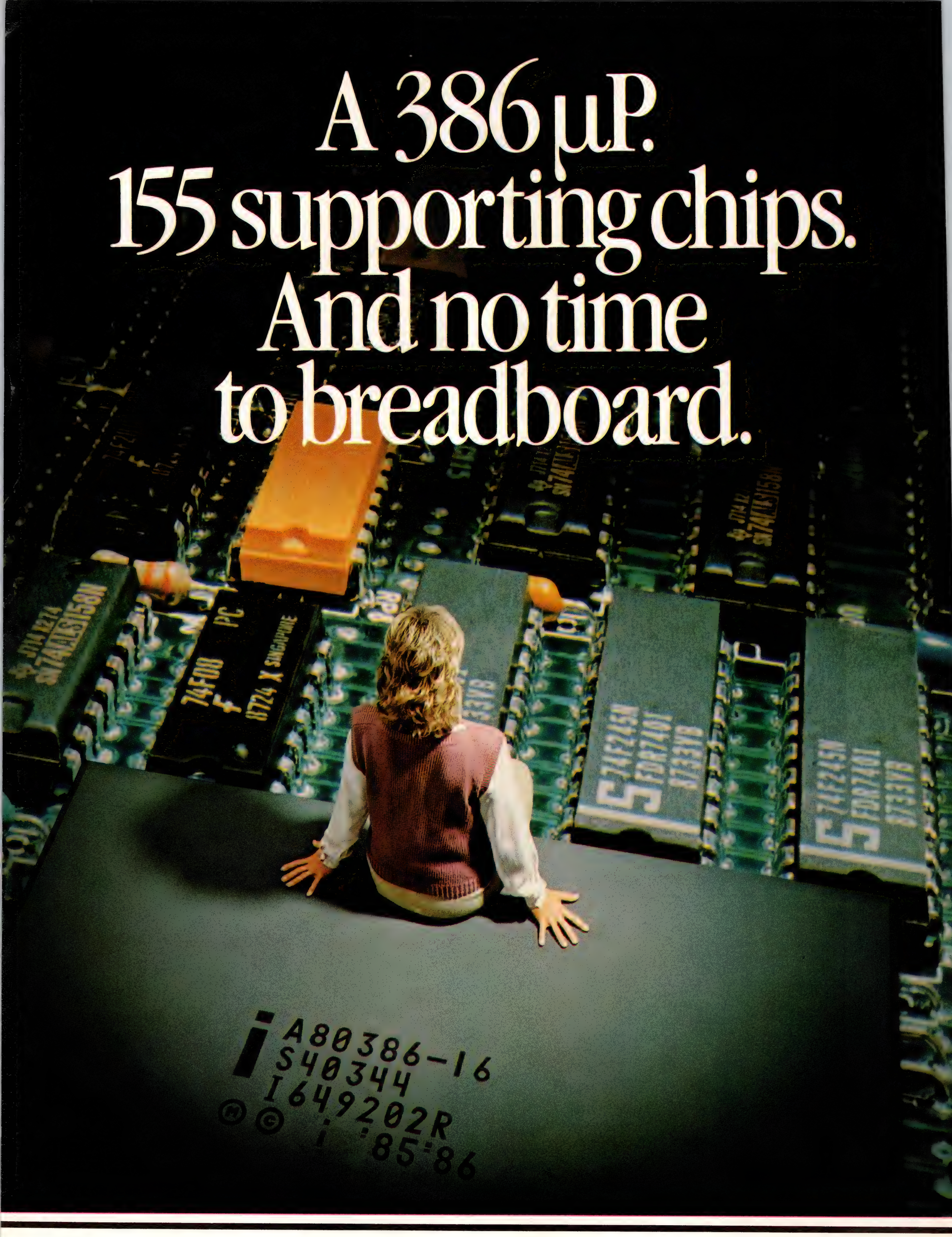
Continued from page 7

EDN Magazine Edition

November 24, 1988


A 386 µP.
155 supporting chips.
And no time
to breadboard.
A80386-16
S40344
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i '85'86

Mentor Graphics lets you simulate an 80386-based motherboard in only 4.3 minutes.

You're designing a complete 32-bit PC motherboard. And you're running out of time.

Your only hope is to bypass the time-consuming breadboard phase and debug directly through simulation. Which means simulating 32 I/O write cycles that program the board's peripheral chips for normal operation — 27,942ns of execution time, including a memory refresh.

So you turn to Mentor Graphics' QuickSim™ logic simulator and run the design file—21 sheets in all, including an Intel 80386 microprocessor and 155 other IC packages, each represented by a SmartModel™ from Logic Automation, Inc.

The result? Simulation completed in just 4.3 minutes.

Introducing the soft breadboard.

With Mentor Graphics, you have a production-proven way to create and debug systems designs—in software. During simulation, design schematics can be displayed, probed, modified, and resimulated. And to complement your simulation, QuickPath™ rapidly checks your design for critical path timing problems. All in a single, interactive work environment.

Your debug operations stay right on your Mentor Graphics workstation, where engineering changes are fast, simple and inexpensive.

Modeling is the key.

Systems simulation requires a wide range of modeling technologies. And that's precisely what we deliver. Like Behavioral Language Models (BLMs), which transcend basic functionality and deliver features such as automatic error detection and reporting. And QuickParts,™ which combine maximum speed with minimum memory requirements—and produce timing behavior identical to the data book.

There's also our Hardware Modeling Library,™ which provides modeling for VLSI parts, including the latest microprocessors. Plus unparalleled support for ASIC libraries, so you can include your ASIC directly in your board simulation.

Once design and analysis is complete, other Mentor Graphics tools follow your design through PCB layout, mechanical packaging, thermal analysis and documentation.

To be continued.

So much for the present. We're already developing new EDA tools for systems design that will extend to every dimension of electronic product development. From high-level systems descriptions to CASE.

It's all part of a vision unique to Mentor Graphics, the leader in electronic design automation. Let us show you where this vision can take you.

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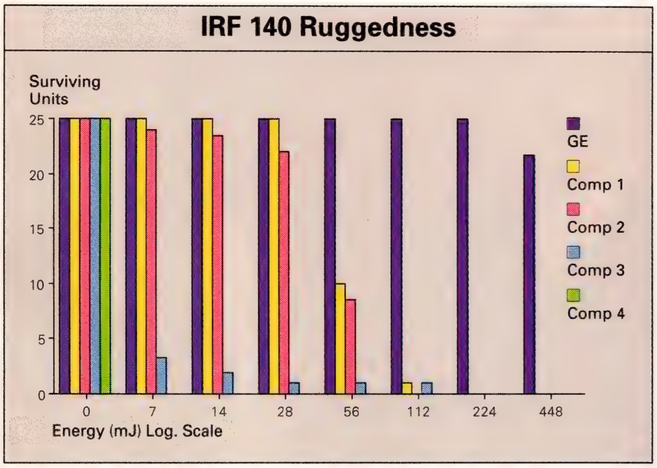
Your ideas. Our experience.

There's an easier way to

make sure it's rugged.

Order GE/RCA Rugged MOSFETs, the only ones with an "R" on the label. Because the wrong device can ruin your creation.

Two years ago an independent testing company compared GE Ruggedized MOSFETs with all leading competitive units. The results were even better than we expected.



In this test conducted by Associated Testing Laboratories, Inc., the ruggedness of 25 GE IRF-series MOSFETs was compared with 25 devices from each of four competitors. As you can see, the GE parts significantly outperformed the others.

Today, the situation is different.

Because our MOSFETs are more than *twice as rugged* as they were then. Yet our ruggedized MOSFETs cost no more than competitors' standard MOSFETs.

A powerful combination.

We've achieved this by combining the rugged technology of GE products with the outstanding manufacturing, quality control and cost-effectiveness of RCA power MOSFETs. So we can bring you the best line of rugged PowerFETs in the industry.

And the benefits are considerable.

Why you need Rugged FETs.

Our Rugged MOSFETs are fast. But they're not fragile.

They're designed, tested and *guaranteed* to withstand a specified level of circuit-induced electrical stress in breakdown avalanche mode.

When you design with our Rugged devices, you can eliminate zener diodes, snubbers and other costly circuitry.

So you save money. And by simplifying your design, you improve system reliability.

Just as important, these devices give you a margin of error.

Because you can never be sure when your system will be subjected to voltages beyond what you expected.

And if you're designing for applications that routinely have to handle surges and transient voltages, these devices are perfect.

A wide selection of drop-ins.

We have more than 200 parts in distributor stock. And they're drop-in replacements for virtually any N-channel devices.

So why take chances, when you can improve your system performance and reliability at no added cost?

For more information, contact your local GE Solid State sales office or distributor. Or call toll-free 800-443-7364, extension 28.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

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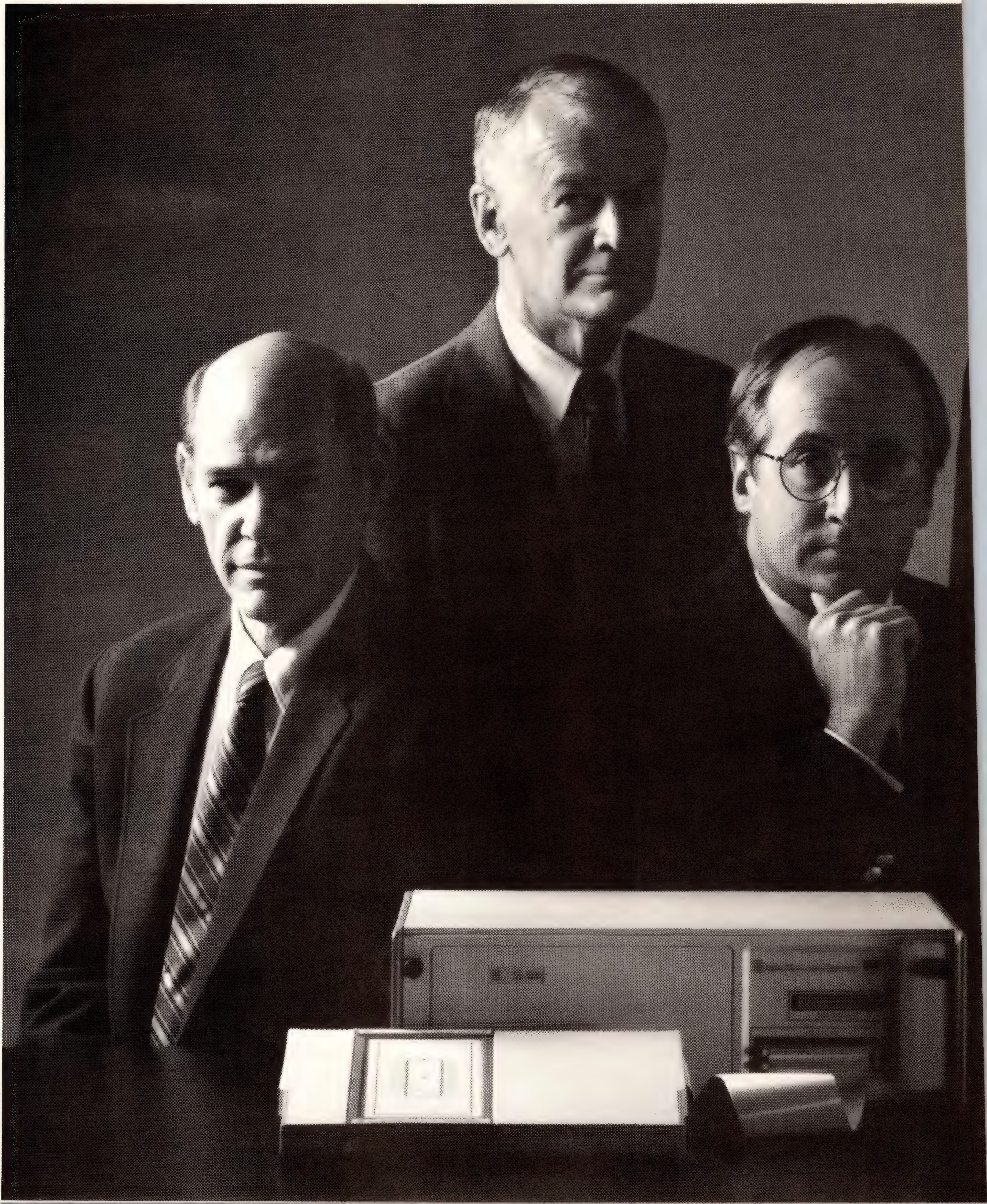


Many are making noise
Fujitsu is turning up the

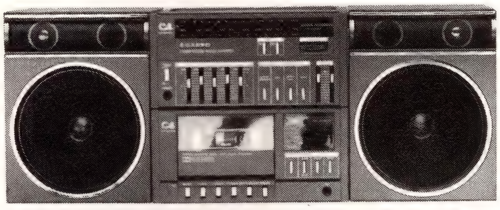
about RISC. But only volume.

Actions speak louder than words.
That's what we believe at Fujitsu. And that's why Sun Microsystems came to us to implement the SPARC™ architecture for the first time. Now, others are finally announcing or sampling their RISC products.

We congratulate them.

But what about their volume production? In the quantities you require for the computers, workstations and peripherals you manufacture.

Knowing how to do it more than once.
It's one thing to produce in the lab — and quite another to do it on the line. Day in, day out. Year after year.



We know, because we've been supplying RISC products in volume since 1986.

Our ability to ship this new technology is a result of many years of manufacturing experience, resulting in Fujitsu's ranking as the world's number one gate array supplier. We're a leading producer of memories as well.

Selecting the architecture that's right for you.
At Fujitsu, we recognize the importance of this key decision to the future of your company.

It can make you — or break you.

That's why we recommend the SPARC architecture of our MB86901 (S-25), and our other RISC devices. It provides a stable, cost effective migration path as we develop successive generations of microprocessors and peripherals to meet your future needs.

SPARC is the only RISC architecture that is available from multiple sources — to minimize your RISC risk. And the only solution that's been proven over time in the Sun Workstation — to guarantee its capability.

32-bits that redefine high-performance.
Our second generation MB86901 high performance CMOS 32-bit RISC processor is available now — in volume. This 15 MIPS, 25 MHz device is just what you need to increase system speed and cut your time to market. And it is supported by a wide range of hardware and software development tools.

Making it happen in Silicon Valley.
Fujitsu's Advanced Products Division is located in San Jose, CA, where all our RISC products, including the MB86901, are designed. So when you do business with us you get the personal attention and technology expertise of Silicon Valley engineering backed by the strength of a $16 billion worldwide organization.

Remember, when it comes to volume — actions speak louder than words.

Fujitsu ships RISC products — now! When you need a lot more than one — we're the only one to call.

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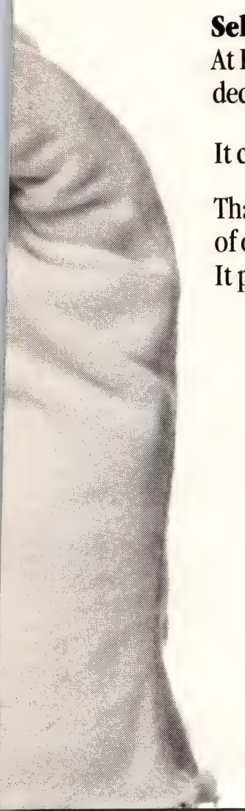

FUJITSU

FUJITSU MICROELECTRONICS, INC.

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CIRCLE NO 106


ECL

You can't catch a rabbit who refuses to rest.

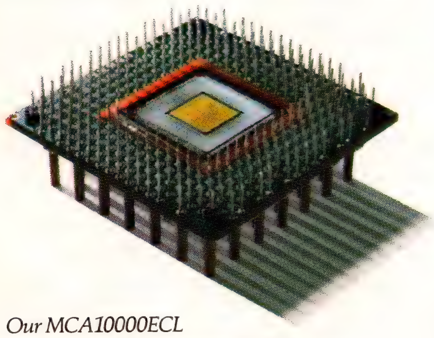
Recently, some ASIC competitors have entered the ECL race and tried to tortoise their way past Motorola's rabbit. Unfortunately for them, they're hoping for a lazy rabbit, while through three generations of ECL arrays the one they're chasing has refused to rest.

So how can they catch an energetic rabbit? They can't.

Performance that won't quit.

Motorola's ECL arrays are the fastest track to total system performance. With speeds of up to 1200 MHz and typical gate delays of 100 picoseconds they're the ultimate in bipolar performance. No longer will designers have to curtail their imaginations to use parts with limited specs.

Motorola ECL arrays not only give you speed and up to 12,402 gates of logic power, they give you the versatility to use them. Programmable speed-power levels put designers in control of both macro and drive currents to allow peak performance where timing is critical and the ability to trim power consumption where speed is less crucial. Three-level series gating lets you multiplex latch inputs without the cost of additional cell usage and delay.



Our MCA10000ECL array is available in a ceramic 235 PGA with 180 I/Os, a polyimide/glass 289 PGA with 256 I/Os, and a 360 lead TAB tape.

Runs faster, cooler and longer.

The MOSAIC III* process used in our third generation ECL arrays utilizes an innovative "edge defined" technique to achieve submicron features without submicron lithography. The end product is very fast—with typical gate delays of 100 picoseconds and metal delays down to 40 ps for a fan out of 2.

An integral heat sink package assures thermal efficiency for reliability and ease of system design. Using impinged air, our packages have a junction-to-ambient thermal resistance of only 2.0°C/W with a forced air velocity of 500 LFPM. This allows high performance arrays to dissipate over 20 watts in an air cooled environment.

Advanced support keeps you race-ready.

To simplify your designs and maximize your potentials, Motorola offers the most comprehensive library available. No longer will you be forced to build system-level functions from a limited selection of library macros and have to accept the loss of performance and density that comes with it. Our library features over 225 functions, three-level series gating, and expandable macros, all of which yield higher performance and better logic density. The library is supported by popular engineering workstations plus a dedicated mainframe which puts even physical layout under your control.

The race doesn't stop.

We know that Motorola has to live up to some pretty tough expectations, after all, we wrote the book on ECL. So we've added a host of innovations designed to make sure your products begin competitive and stay that way. Innovations like tape bonding and STECL outputs.

Multilayer TAB technology provides a controlled impedance environment to minimize interconnect delays. And programmable Series Terminated ECL (STECL) outputs simplify multichip applications.

For more information.

Motorola's ECL arrays provide the most advanced features and the most progressive designs, without ever compromising reliability and the always-important cost/performance ratio.

If you'd like more information about any of Motorola's semi-custom products, contact your local Motorola sales office. For published technical data, just complete and return the coupon below.

We're on your design-in team.

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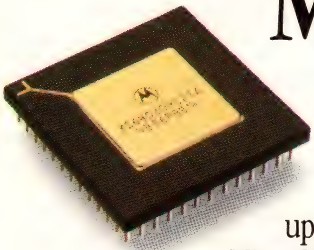
MicroCASE supports the 68030 with 25 MHz emulation.



Step right up to the MicroCASE 68030 PROBE™ In-Circuit Emulator. The first, the fastest, the best 68030 support of its kind.

The 68030 PROBE incorporates the same unique features as our highly successful 68020 PROBE™ —the debugging tool chosen by hardware and software engineers in a wide variety of leading high technology equipment manufacturers world-wide.

Pre-fetch pipeline dequeueing

The 68030 PROBE provides in-circuit emulation— at speeds up to 25 MHz. PROBE also features pre-fetch pipeline dequeueing, so it's easy to figure out which instructions actually execute, and which bus cycles relate to those instructions.

And by merely changing the probe tip, the 68030 PROBE also supports the 68020.

True source-level debugging

The 68030 PROBE provides on-line debugging of high-level language software. Real source statements are displayed, eliminating lengthy translations from assembly language to your high-level language.

PROBE utilizes an IBM® PC AT as its instrumentation chassis, so you can get compiled code to its target via Ethernet, VAXNet, SUNNet, SCSI or RS-232. Whether you compile on a PC, a workstation or VAX,® MicroCASE supports more object code formats than any other vendor.

No need to wait any longer. Real-time emulation and dequeueing for the 68030 and 68020 are available now. From the number one supplier of hardware-assisted software debuggers for the 68000 series. The Atron Division of MicroCASE.

If you'd like more information, or a short product demonstration, call us today at **408-253-5933.** Or circle the number on the reader service card.

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NEWS BREAKS

EDITED BY CLARE MANSFIELD

VARIABLE-FREQUENCY MONITORS SUIT DIVERSE APPLICATIONS

At the recent Comdex/Fall '88 show in Las Vegas, Relisys (Milpitas, CA, (408) 945-1062) introduced two variable-frequency CRT monitors that accommodate varied display formats. The $995 RE1520, an analog color monitor, supports display resolutions to 1024×768 pixels and horizontal-scan rates to 50 kHz. The $499 RM1541, an analog monochrome monitor, supports displays resolutions of 1280×1024 pixels and horizontal-scan rates of 48 to 65 kHz. Both monitors have 15-in. CRTs.

—Steven H Leibson

DESIGN-FOR-TEST ANALYZER EASES PC-BOARD-LAYOUT PROCESS

The DFA (design for accessibility) Analyzer allows you to meet test requirements during the pc-board-layout process. It is part of Valid Logic Systems' (San Jose, CA, (408) 432-9400) Testbridge family of products, which runs within the Allegro pc-board-design system. The analyzer lets you automatically produce board layouts with optimized test-point locations to facilitate access to ATE test fixtures. It includes software for test-point generation, test-document documentation, and numerical-control drill-hole marking. The package will be available early next year as part of Allegro and runs on Sun 3, Sun 4, and DEC VAXstation workstations. The Allegro software starts at $20,000.—Michael C Markowitz

ARCNET CONTROLLER/TRANSCEIVER IC HAS ENHANCED FEATURES

The NCR90C98 Arcnet controller/transceiver chip from NCR Microelectronics Div (Fort Collins, CO, (303) 226-9500) integrates the capabilities of two older devices, the NCR90C26 Arcnet controller and the NCR90C32 Arcnet transceiver. Because these capabilities now reside in one IC, the NCR90C98 can connect directly to the Arcnet cable. The new chip sports improved features such as reduced wait states and an increased capacity (to 8k bytes) for external buffer RAM. It also has added features such as buffer chaining, a power-on reset circuit, and an on-chip oscillator. Available in a 40-pin DIP or a 44-lead PLCC, the device costs $23 (5000).

—Steven H Leibson

PROGRAMMABLE LOGIC DEVICES TARGET ECL DESIGNS

National Semiconductor (Santa Clara, CA, (408) 721-6053) has introduced a family of programmable logic devices for ECL designs. The devices' maximum propagation delay is 4 nsec, and you have a choice of either 10KH or 100KH logic levels. The first two members of the family to be introduced, the PAL1016P4A and 10016P4A, are combinatorial devices. Each accepts 16 input lines and generates 4 output terms with independently programmable logic polarity. The devices operate over the 0 to 70°C temperature range and are housed in 24-pin ceramic DIPs. The PAL1016P4A costs $22.75; the PAL10016P4A costs $25.95 (100).—Richard A Quinnell

PROGRAM HELPS COMPILER VENDORS DEVELOP ADA PROGRAMS

Sun Microsystems Inc (Mountain View, CA, (415) 960-1300) has launched a program to assist compiler vendors in creating Ada programming-language systems for Sun's family of workstations, including the entire line of Sun 3, Sun 4, and Sun 386i computers. According to George Symons, product-line manager for Sun's computer-aided software engineering (CASE) group, no Ada product has become a stan-

dard or won a major market share in the workstation market, and Sun could not find an existing product that met its requirements for an OEM product. Sun developed this assistance program to encourage software engineers to develop Ada for workstations. Through the assistance program, Sun will supply software technology and engineering support to help a partner company couple Ada to Sun's Network Software Environment (NSE) and windowing software.—Steven H Leibson

MODEM SUPPORTS BOTH DATA COMMUNICATIONS AND FAX

The MasterModem communications products from Data Race (San Antonio, TX, (512) 692-3909) combine 9600-bps data-communications and facsimile modems in a single unit. As a data-communications device, the unit operates at 300, 1200, 2400, and 9600 bps and provides MNP level 5 error protection and data compression. The modem supports both asynchronous and IBM synchronous data-communication protocols by employing the Hayes Synchronous Interface (HSI) and Hayes Autosynch protocols. As a facsimile modem, the product communicates with CCITT Group III facsimile machines at 9600 bps, and it can fall back to lower transmission rates automatically when required. You can purchase the MasterModem as a $995 card that plugs into an IBM PC slot or as a $1345 stand-alone device with an RS-232C port. The company also sells a number of software packages for the MasterModems. For example, the firm offers the memory-resident PC-FAX program (a $295 program for transforming an IBM PC into a facsimile machine) and sells a range of IBM synchronous-terminal emulator programs that support one to eight sessions and cost $395 to $595.—Steven H Leibson

1M-BIT DYNAMIC RAM FEATURES 60-NSEC ACCESS TIME

The AAA1M200 Series 1M-bit dynamic RAM from NMB Technologies Inc (Chatsworth, CA, (818) 341-3355) has a maximum access time of 60 nsec, making it the fastest 1M-bit dynamic RAM you can buy. The chips come in 1M-bit × 1 and 256k-bit × 4 versions, cost $20 (100), and will be available in production quantities by the second quarter of 1989. Enhanced-page and static-column mode versions, with access times of 40 and 35 nsec, respectively, will also be available.
—Margery S Conner

DC/DC-CONVERTER FAMILY REQUIRES VERY LITTLE ROOM

Single-in-line packaging allows the BP5000 family of hybrid dc/dc converters from Rohm (Irvine, CA, (714) 855-2131, TWX 910-595-1721) to provide regulated dc power at currents to 1A while consuming minimal pc-board space. The six devices in the family produce 5V, −5V, 12V, or −12V from power supplies ranging from 8 to 20V or 8 to 30V at efficiencies of 50 to 86%. The modules cost $4 to $5 (100); the company also offers them with optional overcurrent protection and output controls.—Steven H Leibson

The Glitch is History

The Glitch won't disturb performance or raise the cost of your design again. Not if you specify TRW LSI's high speed 12-bit DAC. Because our TDC1012 is virtually glitch-free. It settles to ±0.012% of full-scale within 30ns. It operates at data rates to a guaranteed minimum of 20MHz, and reduces spurious harmonics to -65dBc or less, all without need of a sample-and-hold.

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Segmented architecture that replaces the outmoded R-2R ladder, along with several other proprietary design enhancements help account for the TDC1012's record-setting performance. It belongs in your next digital RF, IF or waveform synthesizer, vector graphic display — or anywhere you need a fast, high resolution, distortion-free DAC. It's available now in ceramic or plastic DIP packages from TRW LSI Products or your nearest Hall-Mark or Hamilton/Avnet location. If you need a faster 12-bit DAC, specify our 50MHz TDC1112.

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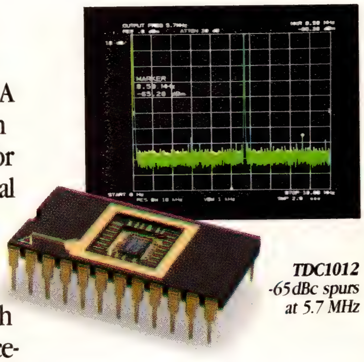

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CIRCLE NO 121

NEWS BREAKS: INTERNATIONAL

V.32 MODEM CHIP SET COPES WITH SATELLITE LINKS

Comprising three dedicated DSP devices, the TS7532 chip set from SGS-Thomson Microelectronics (Agrate Brianza, Italy, TLX 330131; in the US: Phoenix, AZ, (602) 867-6100) allows you to implement the receive, transmit, and echo-canceling functions required in a V.32 (9600-baud) modem. The echo canceler can cope with telephone-line echoes that are delayed by as much as 1.2 sec—the typical delay introduced by two satellite hops. The devices can also compensate for frequency shifts of as much as 10 Hz in the received signal.

The chip set interfaces to the telephone line via the MAFE (modem analog front end) chip set developed by Thomson Semiconducteurs before its merger with SGS. Interfacing to the modem's microcontroller takes place via an 8-bit data/control port. The company is currently working on a software upgrade, which should be available by mid-1989, that will allow you to incorporate other operating modes in the modem—for example, V.21, V.22, V.22 bis, V.23, Bell 103, and Bell 202 modes. The TS7532 chip set is manufactured with the company's 1.2-µm HCMOS-3 process and costs $150 (OEM qty).—Peter Harold

16-BIT CMOS µCONTROLLER SUITS HIGH-END APPLICATIONS

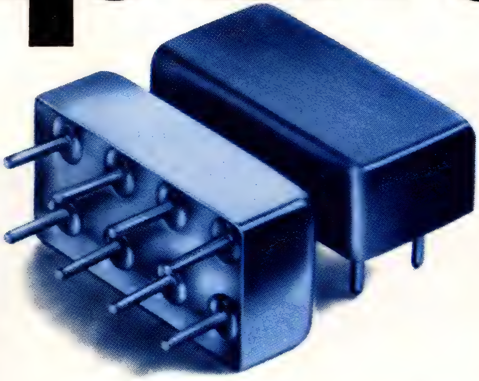
Using its ST9 standard-cell approach to single-chip microcomputer design, SGS-Thomson Microelectronics (Agrate Brianza, Italy, TLX 330131; US contact: Phoenix, AZ, (602) 867-6100) has developed the ST90E30, 16-bit microcontroller. The chip is suitable for use in high-end applications such as automotive and industrial control and telecommunications. The core µP includes a DMA controller, a 16-bit watchdog timer, an I²C- and MSPI-compatible serial interface, and an interrupt handler for the on-chip peripherals and a maximum of eight external interrupts. If required, you can expand the external memory to 120k bytes, at the expense of two of the parallel-I/O ports. Software development tools include a C compiler, macroassembler, linking loader, and software simulator, all of which run on an IBM PC. You have a choice of either a 48- or 64-pin DIP or a 68-pin leaded chip carrier; the LCC version costs $12 (100). A ROM-based version of the microcontroller will be available in 1989 for $5 (500,000).—Peter Harold

SHIFT REGISTERS, DAC TARGET GRAPHICS APPLICATIONS

STC Components' Semiconductor Div (Sidcup, UK, TLX 21836; US contact: Schaumburg, IL, (312) 490-7150) has introduced two video shift registers suitable for use in high-resolution graphics systems. The SLS6016 and SLS6216 each have a 16-bit TTL-compatible latched parallel input port and an ECL-compatible serial output with a 450M-bps data-rate capability (a rate that also makes the devices suitable for high-speed data-link equipment). An ECL-compatible serial input on the front end of the shift registers allows you to cascade devices to accommodate greater word widths, and additional control inputs allow you to implement hardware zoom and scroll functions. The SLS6016 operates from a −5.2V supply and requires TTL input levels referenced to the negative-voltage supply. The SLS6216 operates from 5V and −5.2V supplies, allowing you to drive its TTL inputs from logic circuitry powered from a 5V supply rail. Both video shift registers sell for around £10 (100).

The manufacturer also intends to offer the SCD6038 triple 8-bit video DAC during the first half of '89 at a price of around £40 (100). Like the video shift registers, the D/A converter also suits high-resolution graphics systems. It is pin compatible with other manufacturers' devices, but will have a clock frequency of at least 250 MHz and typical power dissipation of only 1.7W.—Peter Harold

rugged plug-in amplifiers



0.5 to 1000MHz from $13.95 (10 to 24 qty)

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MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
★MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †IdB Gain Compression ◇Case Height 0.3 In.
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LOW PASS Model	*LP-	10.7	21.4	30	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to		10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max, 20dB Stop Frequency (MHz)		19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

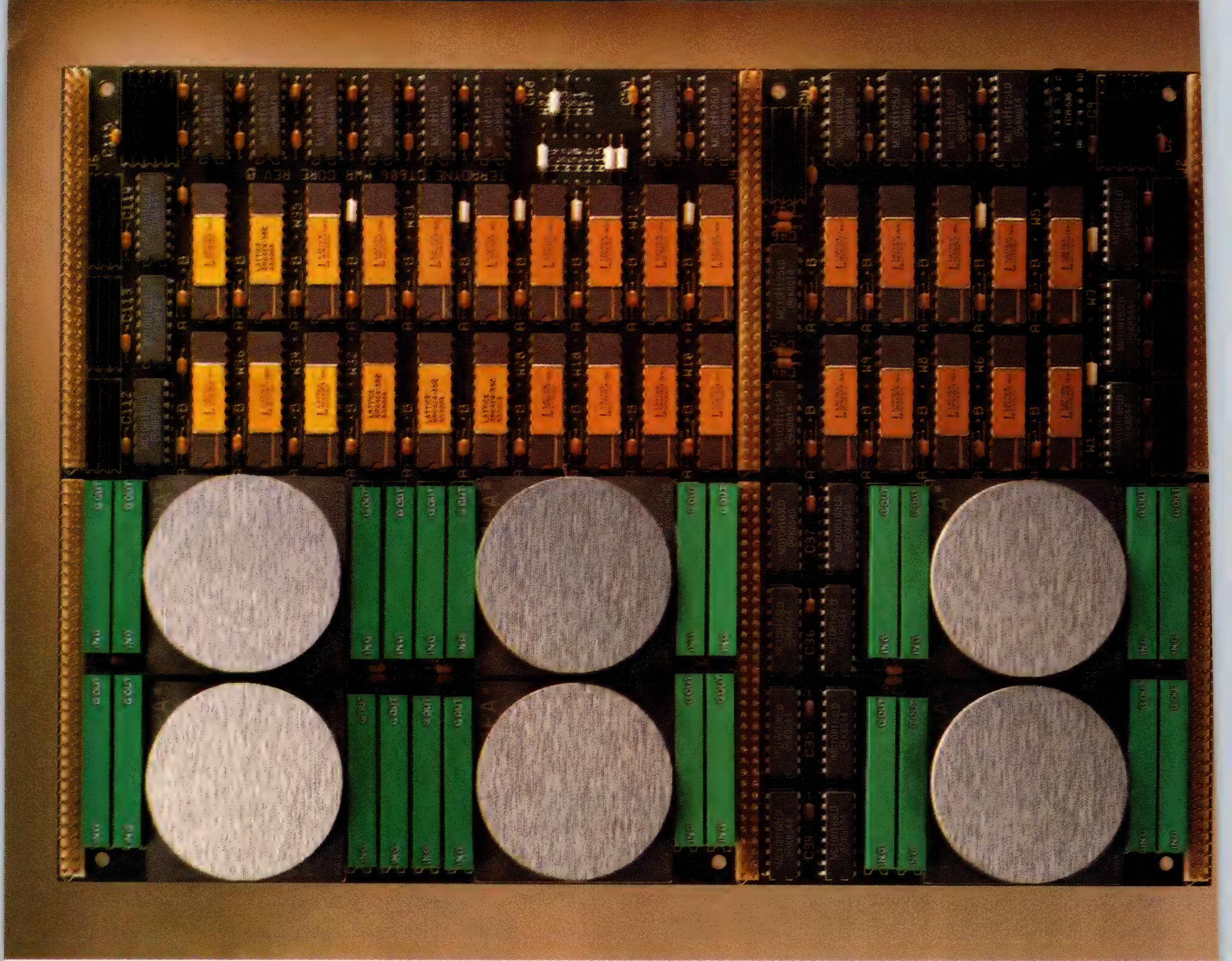
Prices (ea.): Qty. (1-9) P $11.45, B $32.95, N $35.95, S $34.95

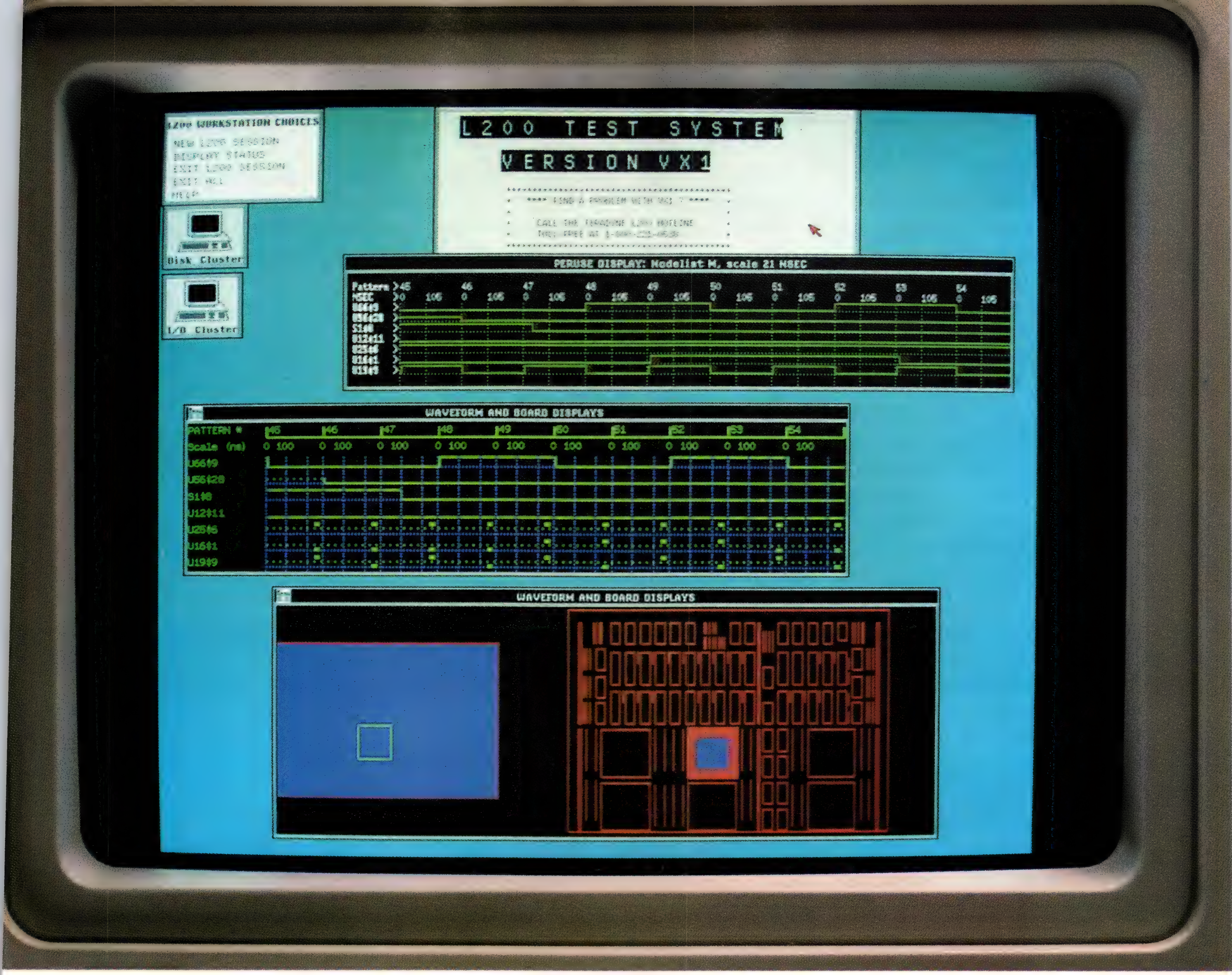
HIGH PASS Model	*HP-	50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)	start, max.	41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)		26	55	95	116	150	190	290	365	460	520	570	660	720

Prices (ea.): Qty. (1-9) P $14.95, B $36.95, N $39.95, S $38.95

*Prefix P for pins, B for BNC, N for Type N, S for SMA   *example:* **PLP-10.7**

C105 REV. E





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CIRCLE NO 122

US should stop protecting its competitors

Jon Titus's editorial "Spend it here" (EDN, August 4, 1988, pg 49) was on the right track until it derailed on a common copout.

The answer to cheap Far East imports is not to impose tariffs. In his editorial, Titus says that "in most cases" tariffs are counterproductive. Tariffs transfer money from consumers to slow-moving bureaucrats to whatever special interests happen to be in political favor at the time. Let's face it, tariffs are *always* counterproductive.

The reason that Japan, Korea, and Taiwan have such deep pockets is that they are reaching into the pockets of the American taxpayers. Forty years ago, US military forces were sent to protect those countries while they recovered from the ravages of war. Now the babies are fully grown and are sitting on their babysitter, yet they still demand protection.

US manufacturers and their employees are being forced to shell out billions of dollars to subsidize their competitors. *That* is the money that should be spent here.

The answer to unfair competition is to level the playing field. Let's stop subsidizing our competitors. Bring US military forces home where they belong, and leave the political bureaucracy out of the loop.

John Parsons
El Segundo, CA

US government should set support prices for US ICs

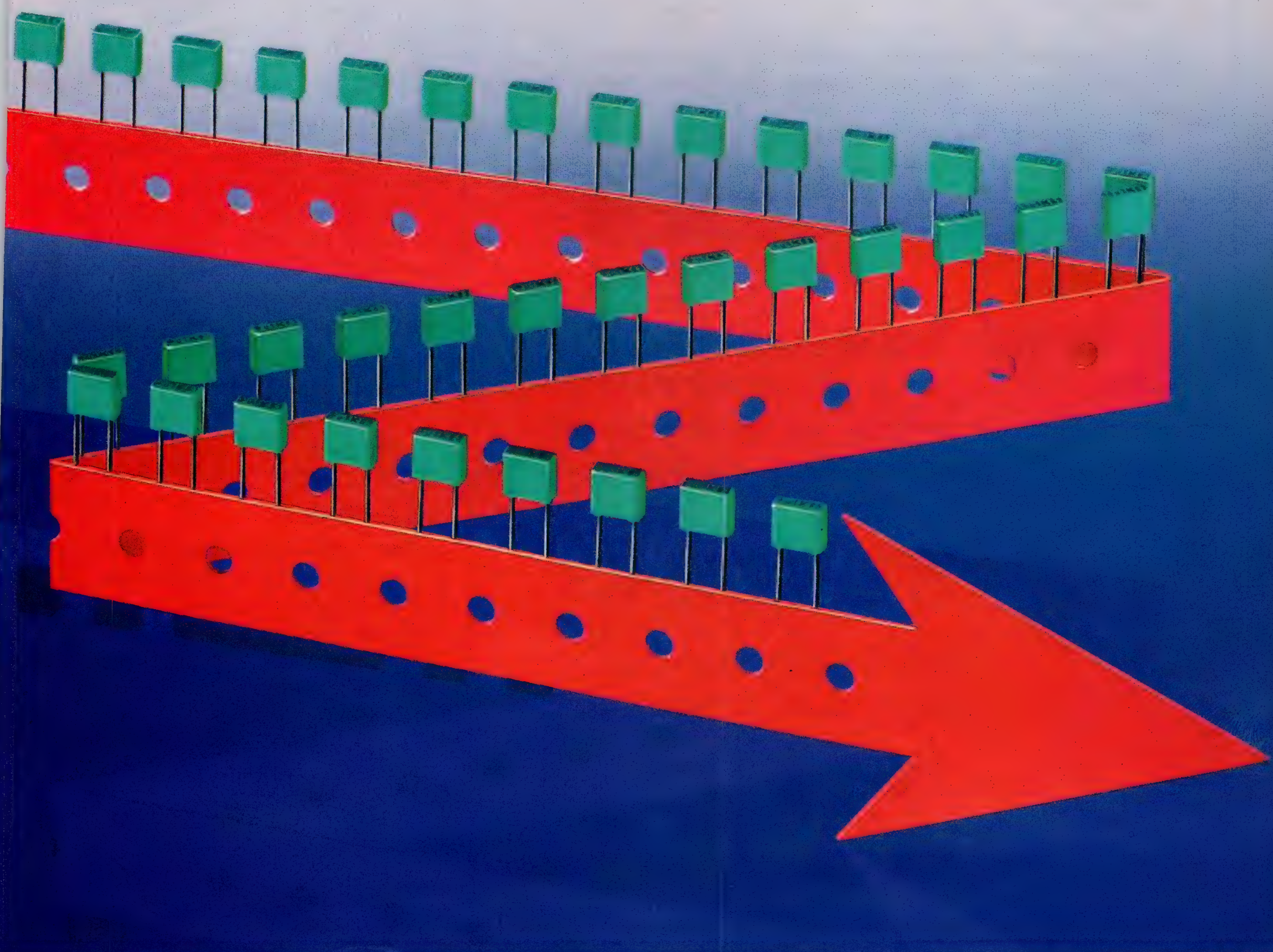
I agree with Jon Titus that the 1986 semiconductor pact was illogical and shortsighted. Forcing foreign suppliers to charge us more for their products is idiotic.

But the solution proposed in the editorial ("Spend it here," EDN, August 4, 1988, pg 49) is no better. A tariff on DRAMs still keeps their price higher than that of DRAMs on the free market and makes all US-manufactured goods using them cost more. That makes it more difficult for us to compete in foreign markets.

If we need to shelter the US IC industry for a good reason (it's deserving of charity, it's essential to national defense, US laws do not allow it to compete fairly with foreign firms, etc), then we should do as we do for farmers.

Let the government set support prices for US-made ICs. If they can't be sold at the support prices, the government buys them and stores them along with the butter and cheese.

Had we done this in 1986, the government would have lots of



DRAMs in storage by now. It could sell them off, thus preventing a shortage. And we'd all be paying 1986 prices for them.

Jack Althouse
Palomar Engineers
Escondido, CA

Design Idea corrections

Please note the following corrections to the Design Idea "Time-delay relay has quick release" by John A Haase (EDN, July 21, 1988, pg 329). The third paragraph states that "the voltage at C_3 then subsides to an equilibrium value (3V) . . . ." The sentence should read: "The voltage at C_2 then subsides to an equilibrium value (3V) . . . ."

Further, the author notes that the circuit is versatile enough to operate from an untapped secondary. "If you don't have a center-tapped winding," he says, "simply omit D_5 and short-circuit R_4."

New price

The News Break on the TR9C1640 and TR9C1643 static RAMs from Triad Semiconductors (EDN, September 15, 1988, pg 24) contained an error: The prices listed didn't jibe with the speed ratings. What's more, the manufacturer has since changed the prices. The 25-, 35-, and 45-nsec versions of both parts now cost $13, $10, and $9 (1000), respectively.

Phone home

The telephone number given for Signetics Corp in the Product Update "Video and system controller IC promises low-cost 16/32-bit color computers" (EDN, August 4, 1988, pg 83) is incorrect. The correct number is (408) 991-2000. The number published in the article, (408) 991-4571, is now the company's FAX number.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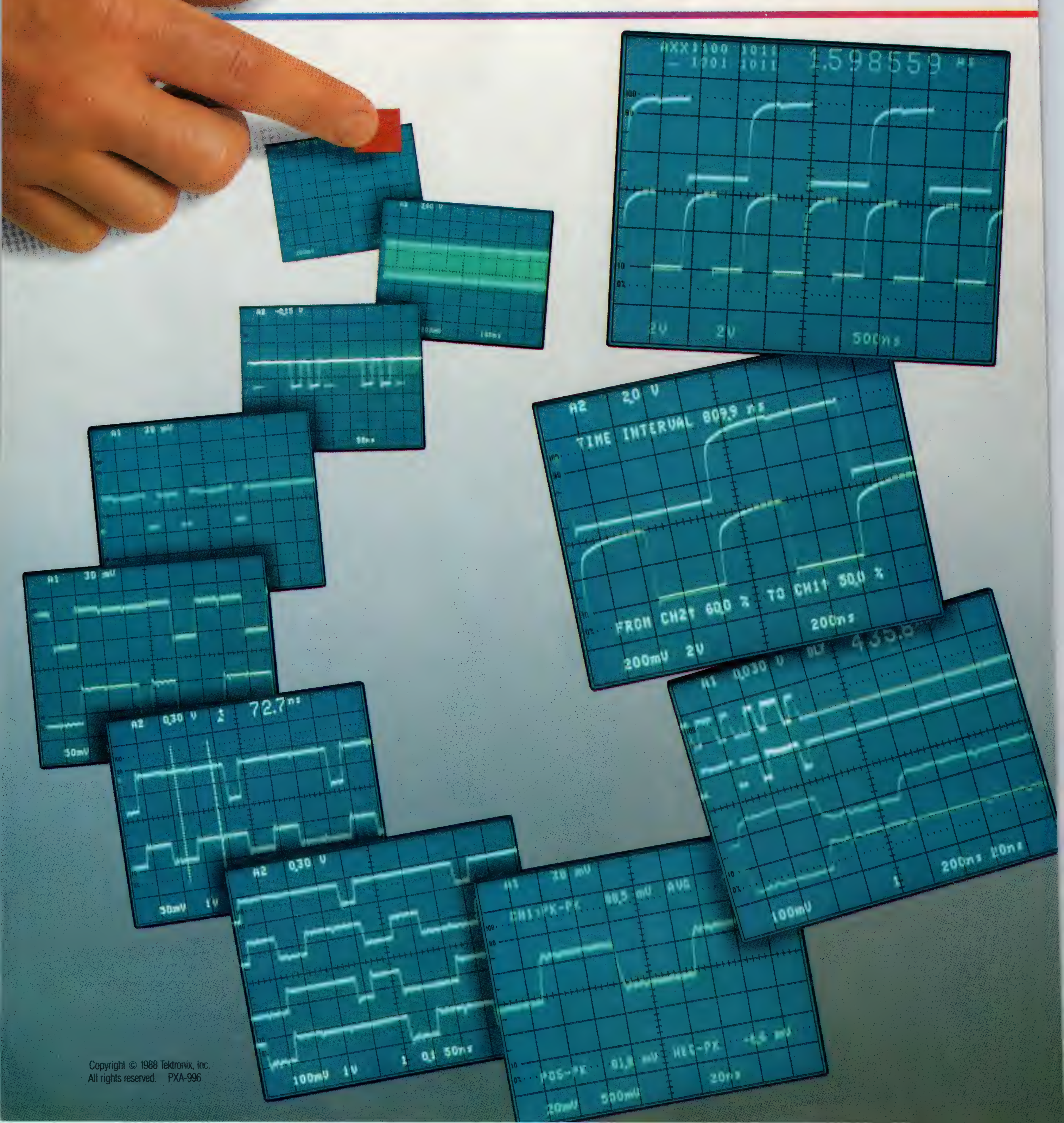

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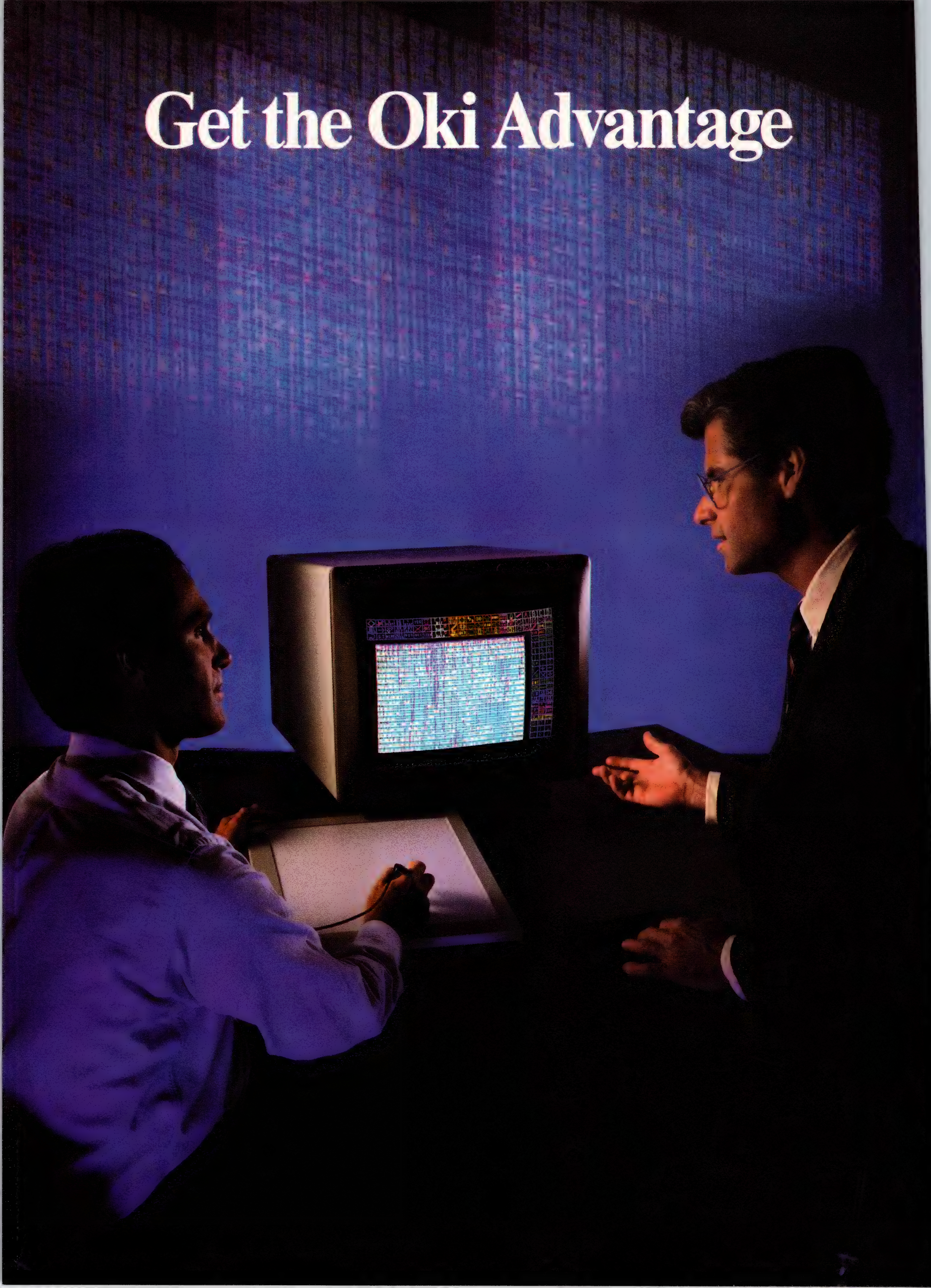
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CALENDAR

CASE: A Manager's Guide (seminar), Washington, DC. Technology Transfer Institute, 741 Tenth St, Santa Monica, CA 90402. (213) 394-8305. December 6 to 8.

Software Quality Assurance & Testing (short course), San Diego, CA. John Valenti, Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (231) 417-8888. December 7 to 9.

Fourth Aerospace Computer Security Applications Conference, Orlando, FL. IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. December 12 to 16.

Programming and Interfacing the IBM PC for Data Acquisition and Control (short course), Orlando, FL. Purdue University School of Engineering and Technology at Indianapolis, 799 W Michigan St, Indianapolis, IN 46202. (317) 274-0806. December 12 to 16.

US-Hong Kong Technology Business Conference, Hong Kong. Asian American Manufacturers Association, 800 Menlo Ave, Suite 115, Menlo Park, CA 94025. (415) 321-2262. December 19 to 23.

Real-time System Design: A Hands-on Workshop (short course), Washington, DC. John Valenti, Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (231) 417-8888. January 10 to 13.

SC Global 89, San Francisco, CA. Superconductor Applications Association, 24781 Camino Villa Ave, El Toro, CA 92630. (714) 586-8727. January 11 to 13.

OE LASE '89, Los Angeles, CA. Society of Photo-Optical Instrumentation Engineering (SPIE), Box 10, Bellingham, WA 98227. (206) 676-3290; in Europe: SPIE, Koblenzer

CALENDAR

Strasse 34, D-5300 Bonn 2, West Germany, 49-228-36-15-46, TWX 172-283-747. January 15 to 20.

Fifth Annual Computer Graphics New York Show, New York, NY. Exhibition Marketing & Management Co, 8300 Greensboro Dr, Suite 110, McLean, VA 22102. (703) 893-4545. January 17 to 19.

The 1989 Optical Disk Systems Conference: From the Mail Room to the Board Room, Phoenix, AZ. CAP International Inc, 1 Longwater Circle, Norwell, MA 02061. (617) 982-9500. January 23 to 25.

ATE & Instrumentation Conference West, Anaheim, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. January 23 to 26.

Winter 1989 Unix Technical Conference, San Diego, CA. Usenix conference office, Box 385, Sunset Beach, CA 90742. (213) 592-1381. January 30 to February 3.

Electromagnetic Interference—Characteristics and Control (seminar), Center for Continuing Engineering Education, University of Wisconsin-Milwaukee, 929 N Sixth St, Milwaukee, WI 53203. (414) 227-3120. January 31 to February 2.

Power Electronic Conference '89, Santa Clara, CA. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06854. (203) 852-0500. February 7 to 9.

Software Development '89, San Francisco, CA. Miller Freeman Publications, 500 Howard St, San Francisco, CA 94105. (415) 995-2471. February 14 to 17.

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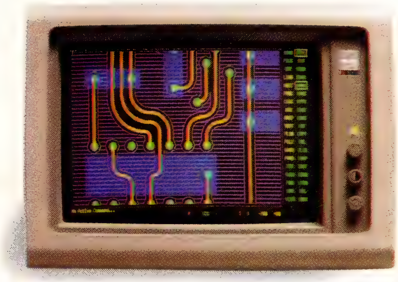

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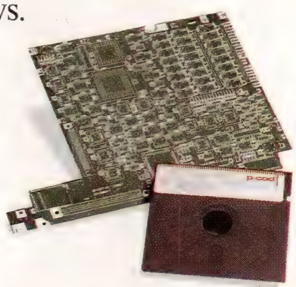

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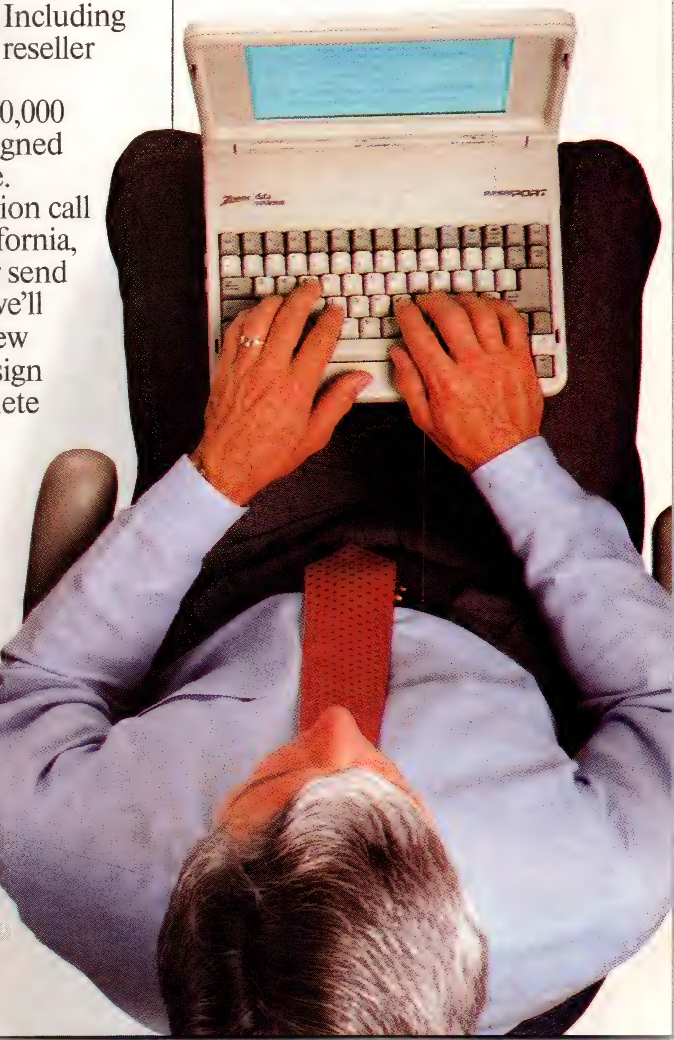

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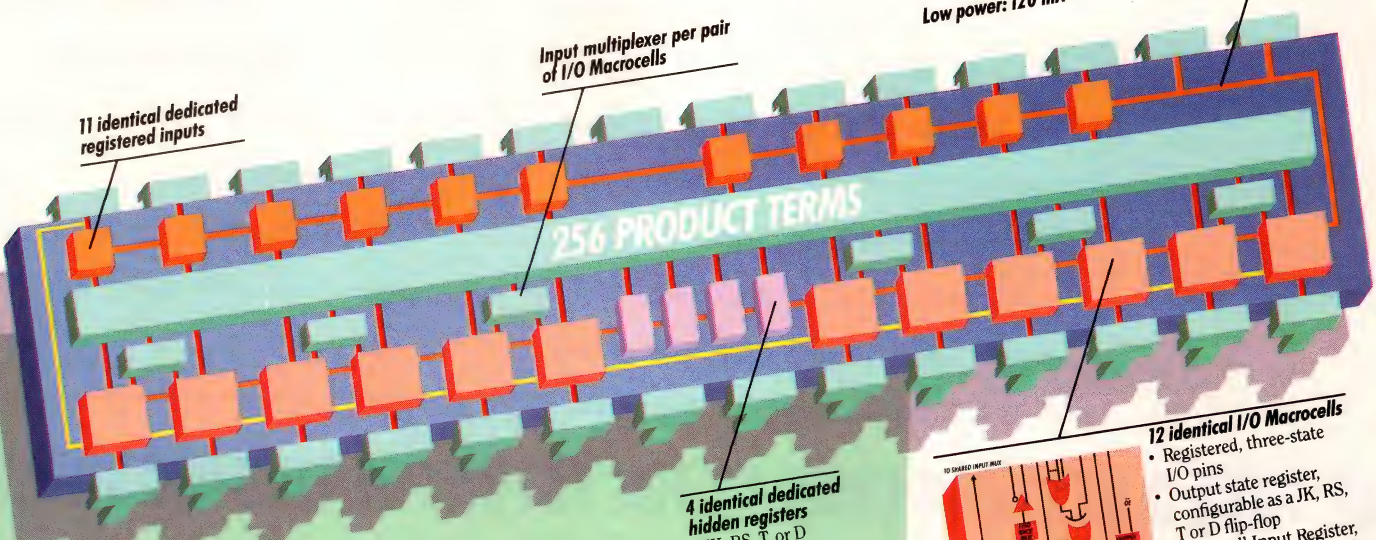

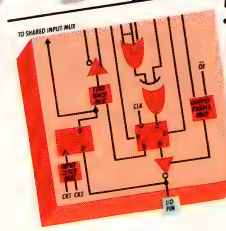

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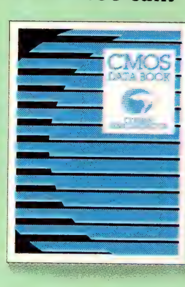

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EDITORIAL

Software designers have it easy

I've enjoyed both writing programs and designing circuits, and I always assumed that the difficulties in both pursuits were roughly equal. However, the people who design software may lead pretty easy lives. At least, that's what Brady Barnes of Inter-Tel (Chandler, AZ) recently wrote to say. He has written assembly-language programs and has designed communication circuits, so he has seen both sides of the hardware/software world, too. Here's the gist of Brady's letter:

All too often, hardware engineers find that delivery times for critical parts are too long, so they must select replacements or redesign their circuits. On the other hand, programmers don't complain, "Yeah, the LDXA op code has a 16-week lead time, so I have to rewrite all my code." Then there are manufacturing considerations, too. The production people may say that they can't produce a circuit because their equipment won't insert radial-lead capacitors on 0.1-in. centers. For the engineer, it's back to the CAE system. On the other hand, programmers aren't heard to complain, "The PROM programmer doesn't like JMP op codes, so we have to strip them out and use conditional branches instead."

Environmental testing can throw a few curve balls at hardware designers, too. Crank up the test chamber to 70°C and watch the circuit stop functioning when a critical timing relation you forgot about causes havoc. Few software engineers worry that their programs will fail at high temperatures. Government rules and regulations are another story. Although communication gear may have to pass FCC Part-68 or UL tests, communication algorithms have no such restrictions.

Cost is another issue that frequently drives hardware designers crazy. In an effort to save a few cents here and there, someone may decide to substitute one part for another—say, 5%-tolerance resistors for 2% units. Yet few programmers are ever told, "Let's save a few cents and cut out those expensive NOP instructions."

The hardware-vs-software battle goes on even after the company introduces the product. A typical product announcement may play up the software, its wonderful user interface, its high speed, and its versatility ad nauseam, while ignoring the hardware. The ultrasophisticated, state-of-the-art hardware gets a throw-away line in the marketing presentation, while the software—which is full of minor bugs and which will undergo seven revisions—steals the show.

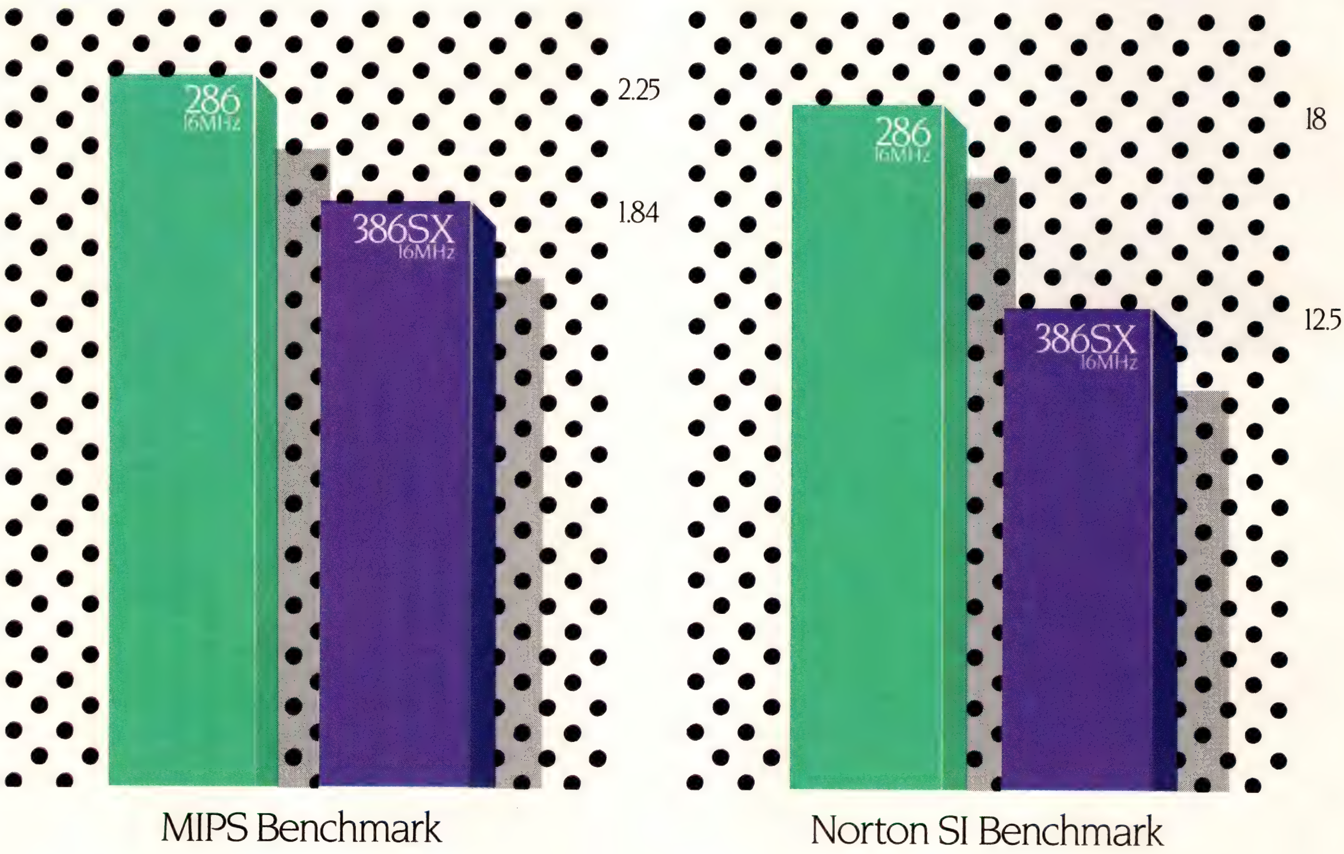
Brady makes some interesting points, but programming never seemed that easy to me. Back in the early days of the microprocessor, I heard of one programmer who followed each jump instruction with a halt command. He just couldn't trust the jump instructions to operate properly and wanted to be sure the CPU's circuits wouldn't "ignore" one and continue through the program in an uncontrolled way. So, programmers have their own "hardware" stories to tell, and I'm eager to hear them.

Jon Titus

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981

The 386SX: Good who want slower,



All benchmarks performed with an Everex Step 286-16 with 0 wait states and a Compaq Deskpro 386S™ with 0 wait states. Both systems running 16-bit DOS and OS/2 software. Dhrystone 1.1 compiled with Microsoft® C compiler with no optimization. Run under DOS 3.31. Norton SI by Peter Norton Computing, Inc. performance reported relative to an IBM PC-XT.® MIPS written by Chips and Technologies. Chip cost based on 1000 piece quantity. Product names mentioned herein may be trademarks and/or registered trademarks of their respective companies.

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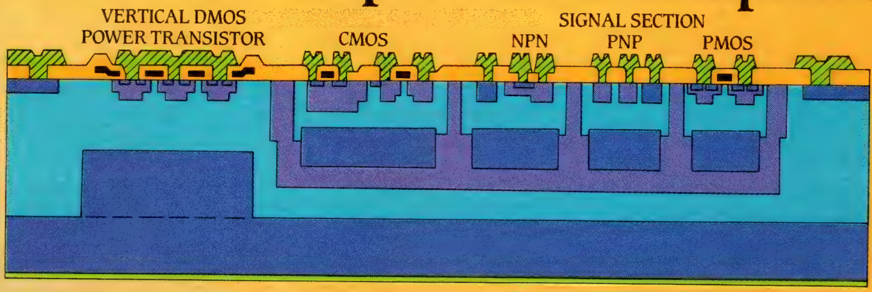

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New ICs speed laser-printer control

Your choice of a laser-printer controller IC will depend on more than just the ICs' specs. The page-description language, the type of printer you're designing, and the speed/cost tradeoff will be big factors in your selection process.

Margery S Conner,
Regional Editor

Although the print mechanism (or print "engine") of a typical laser printer can operate at a minimum of 8 pages/minute, the time it takes for the control electronics to construct the page and send it to the engine may push the actual print time closer to 8 minutes/page. If you're designing the control electronics for a state-of-the-art laser printer, you'll certainly want to improve on that speed. Fortunately, you can now obtain a variety of ICs, from stand-alone RISC processors to support-function ASICs, that can both speed the operation of the printer-control electronics and reduce their cost and the board space they require. Two key aspects of laser-printer-controller design should guide your choice of a control IC: the control language your printer will use and the speed at which the printer must run the language.

Fig 1 shows the basic scheme for a laser-printer controller board. The user of the printer determines what the page to be printed will look like by using an application program such as a desktop-publishing or CAE package. The application program builds a list of page-description language (PDL) commands, which it sends to the printer's control-electronics board, and the board builds an image of the page in its bit-mapped RAM. The video interface sends the bit map out to the print engine, which actually prints the page.

The bottleneck in this process is the time it takes the processor to create the bit map with the commands from the application program. All laser-printer controllers are commanded by the application program in one of several PDLs. The PDL's complexity is probably the major factor in determining how fast the printer will run.

This evaluation system includes *the XL-8200-40 raster-printer-controller board, the printer-interface module, Weitek's Postscript-compatible interpreter, and documentation. It's priced at $15,000.*

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Printer-control ICs

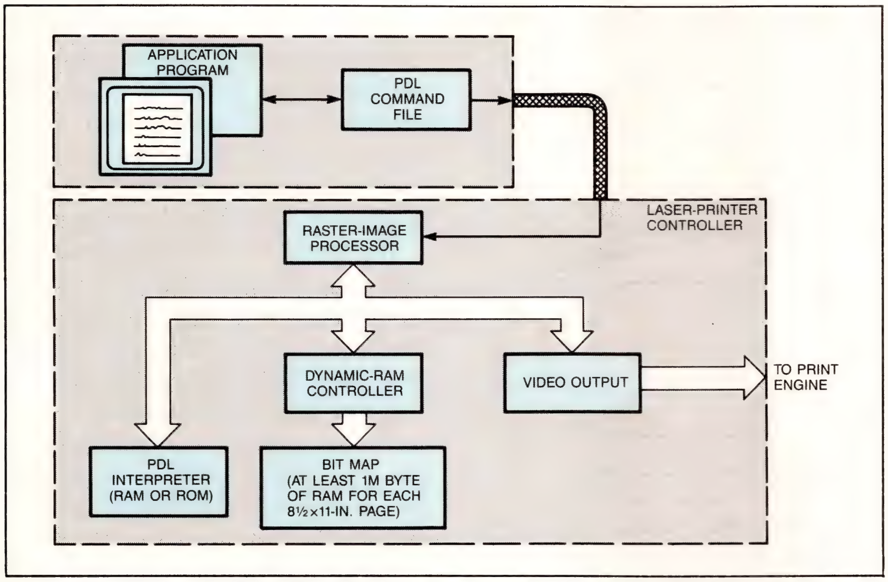

***Fig 1—An application program such as a desktop-publishing or CAE program communicates** the page makeup to the laser-printer controller by using a page-description language (PDL). The raster-image processor uses the PDL commands to build a bit-map image of the page. The processor sends the bit-map image through the video-output section to the print engine. The two main features that distinguish controller chips are their overall capabilities and the amount of peripheral capability (such as DRAM and video control) they include.*

Most laser printers use one of two languages: Hewlett-Packard's relatively simple PCL (printer-control language), or Adobe Systems' much more complex Postscript. Several companies offer Postscript-compatible languages.

The simpler PCL stores the font as a bit map. It's difficult, if not impossible, for the processor to manipulate the font as a bit map, and the fonts consume large amounts of memory. Keep in mind, however, that the vast majority of work performed on laser printers is simple text in one font style. For this reason, most laser printers are currently based on PCL, and it's likely that at least half of the laser printers that are introduced in the next two years will also use PCL-like languages.

Powerful PDLs

Postscript and Postscript-compatible languages are more powerful and complex than PCL because they store fonts algorithmically, rather than as bit maps. Algorithmically stored fonts comprise a series of control points and the equations for the curves (they're often Bezier curves) that link the points. Because the fonts are stored as algorithms, the controller can rotate them, shrink them, change their aspect, and otherwise manipulate them by performing a transformation on the basic font. All this power comes at a price: Postscript-compatible languages require a great deal of processing time. Further, Postscript is readable in ASCII form, which is a big advantage in developing code, but which requires additional processor-interpretation time.

Another advantage of Postscript software is that it's device independent: Software written for one Postscript-compatible printer will run on all the printers. This device independence requires even more processor overhead.

The combination of device independence and programming power makes Postscript a very attractive language for relatively high-end laser printers. Printer-controller ICs can help make Postscript practical because they speed the processing of the language.

The IC manufacturers have taken two different tacks in developing laser-printer-control ICs: Cirrus Logic, National Semiconductor, and Weitek each developed a processor or coprocessor optimized for graphics and printer-control functions; Western Digital and Personal Computer Products offer ICs that basically consist of interface logic for specific processors, and circuitry that performs such functions as video and DMA control. In addition, some more general-purpose processors such as Texas Instruments' 34010 graphics processor are also suitable for laser-printer control.

Cirrus Logic's GP340 is a low-priced coprocessor—it costs \$25—that you can use with a low-priced general-purpose μP such as the 68000. (Almost all of the current low-end laser printers are based on the 68000.) Using the 68000 gives you two advantages. First, the μP is inexpensive, selling for as little as \$5 in OEM quantity; second, it has a wide existing base of software.

The GP340 can build the bit map with hardware-assisted bit-block transfers (BitBlts), scan the bit map out to the print engine, and perform dynamic-RAM refresh and control. Although Cirrus claims that the coprocessor can support print engines that operate as fast as 40 pages/minute, keep in mind that the 68000 processor can't support this speed, because the chip is simply too slow. To obtain a high print speed, therefore, you'll need to use a more powerful processor, such as a 68020, which costs about \$100. You could use other high-performance, general-purpose processors, but you probably won't want to, because they're equally or more expensive and they don't have an existing base of laser-printer-control software.

Printer-control ICs

National Semiconductor's and Weitek's controllers are powerful, dedicated processors. National Semiconductor's 32CG16 is based on the company's general-purpose, 32-bit 32000 processor family and uses a superset of the 32000's commands. The additional commands support on-chip BitBlts. The chip costs $20 in OEM quantity. Because the 32CG16 is based on the 32000, you can use all of the family's support chips with it. The NS32CG821, for instance, provides dynamic-RAM control; the NS32081 handles floating-point math; and the DP8510 performs BitBlt acceleration. These support chips cost $7.25, $35, and $5.25, respectively.

Weitek's XL-8200 2-chip set is a RISC (reduced-instruction-set computer) processor that comes in different speed versions to match the speeds of different print engines. The -10 version supports 10-page/minute engines and costs $99 (50,000); the company also offers the -20, -40 and -60 versions, which support 20-, 40-, and 60-page/minute print engines and cost $149, $199, and $299, respectively. Each chip is a 145-pin CMOS device in a pin-grid array.

Another factor that you'll need to consider in selecting a printer-control IC is the manner in which the chip performs BitBlts. Printer-controller ICs use BitBlts to transfer fonts from the font cache to the bit map.

In general, printer users obtain fonts on nonvolatile storage media, such as floppy disks. Most printers have a section of memory called the font cache, where the processor loads the fonts upon power-up rather than waiting until it's actually composing the bit map to pull the fonts in from the floppy disk. To move the fonts into the bit map, the processor logically ORs the source block of data with the destination data and stores the result in the destination address. This procedure is an example of a 2-operand BitBlt. Three-operand BitBlts are similar, except that the source data is logically operated on by a texture or pattern, and the results are stored in the destination location. The 3-operand BitBlt operation is commonly used to perform such tasks as incorporating a patterned background in a window area, for example.

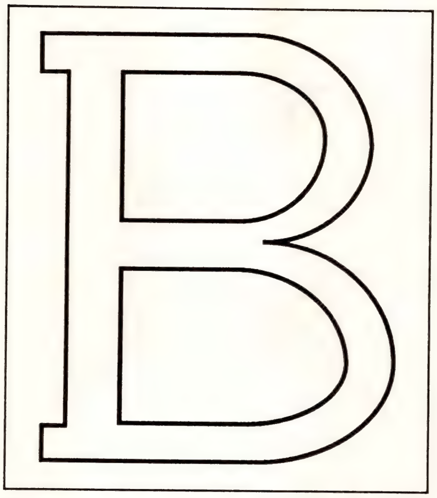

Fig 2—This letter B is shown in a font type commonly used by laser printers. *A Postscript-like PDL develops the bit map for a font type's character set by using a series of control points to bias the Bezier curves according to the equation* $x,y=at+bt_2+ct_3+2dX$. *Calculating the character set requires 20 floating-point calculations/point×20 curves/character×250 characters/set×87 points/character, which equals 8.7 million computations for each character set.*

BitBlts are also the easiest PDL functions to accelerate in hardware. The Cirrus, National Semiconductor, and Weitek chips all offer different schemes for performing BitBlts.

Cirrus's GP340 coprocessor, for example, implements BitBlts in hardware. While the CPU is building the display list of commands or running the PDL, the coprocessor can fetch a BitBlt command and source and pattern data from the display list, perform the BitBlt, and write to page memory without CPU intervention. The Cirrus chip's strength is that it performs BitBlts in hardware, a feature that makes it suitable for printers that must generate a large quantity of text as opposed to graphics. (Although printer manufacturers often boast about their printers' graphics capabilities, the majority of a printer's workload is actually printing text.)

National Semiconductor's 32CG16 supports on-chip BitBlt commands, and also interfaces to the optional DP8510 BitBlt processing unit (BPU). Neither the processor nor the BPU implements 3-operand BitBlts; to effect a 3-operand BitBlt, you'll need to perform two 2-operand instructions serially.

Although it doesn't perform BitBlts in hardware, the Weitek processor doesn't sacrifice speed. In keeping with the RISC principle, the chip doesn't have any complex BitBlt instructions; rather, you use the bit-field operations to develop your own BitBlts. You don't have to develop your own BitBlts, however: The software package supplied with the chip includes a Postscript-like language that supports BitBlts.

Billions of calculations

To display fonts, the processor in a Postscript-compatible printer must do more than simply copy the fonts to the bit map; it must first create the fonts. Basically, the fonts consist of control points and algorithms that tell which pixels are turned on between the control points. Determining these dots for even 300-dpi resolution requires many calculations; Weitek estimates that a simple page with only one or two fonts may require 2 million calculations; a complex page may take billions (**Fig 2**). To implement Postscript-compatible commands at high speeds, you'll need a floating-point unit (FPU).

The GP340 makes no provisions for an FPU; you have the option of using whatever FPU or math coprocessor is available for the gen-

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This past June, Hewlett Packard became the first major U.S. computer manufacturer to introduce a workstation system based on Motorola's 68030 32-bit microprocessor.

As expected, it's turned out to be quite a system. The HP 9000 Model 360, in fact, reaches processing speeds of up to 5 MIPS at 25 MHz. And the new Model 370 hits over 8 MIPS at 33 MHz.

Largely due to Motorola's 030. After all, it delivers more performance than any other conventional microprocessor on the market today, and even outruns a number of RISC* processors. Plus it offers firsts like on-chip data and instruction caches, parallel architecture and unique DRAM interface.

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eral-purpose processor you use. The 32CG16 and the XL-8200 both offer FPUs as an option. National Semiconductor's NS32081 FPU adds $35. Weitek offers an FPU with the XL-8200 and sells the combination as a 3-chip set (the XL-8232); you pay about a 60% premium for the FPU. Even without the FPU, the RISC chip set can perform a 32-bit floating-point multiplication in eight cycles.

If you try to compare printer-controller ICs merely on the basis of their specifications—such as whether they have FPUs and whether or not they perform BitBlts in hardware—you may not select the chip that best suits your application. Many other factors also affect the speed at which a laser printer can run. Laser-printer resolution and control languages and a bit map's memory type and speed, for instance, all vary considerably—and they all affect the print speed (see **box** "Two designs highlight ICs' bit-mapping speed").

Unlike Cirrus, National Semiconductor, and Weitek, which developed their processor/coprocessor chips to accelerate processing functions in hardware, Western Digital and Personal Computer Products Inc developed chips that incorporate the support circuitry for a 68000 processor. These chips don't include any hardware BitBlts, nor are they accessed via a display list.

Two designs highlight ICs' bit-mapping speed

You can't come up with one figure of merit for comparing printer-controller ICs; you need to consider many factors. The ICs' performance is highly dependent on the applications you design them into. Two big differences you'll notice among controllers are the time it takes for the printer-controller electronics to create the bit map, and the cost of the components you need to design into the printer-controller board.

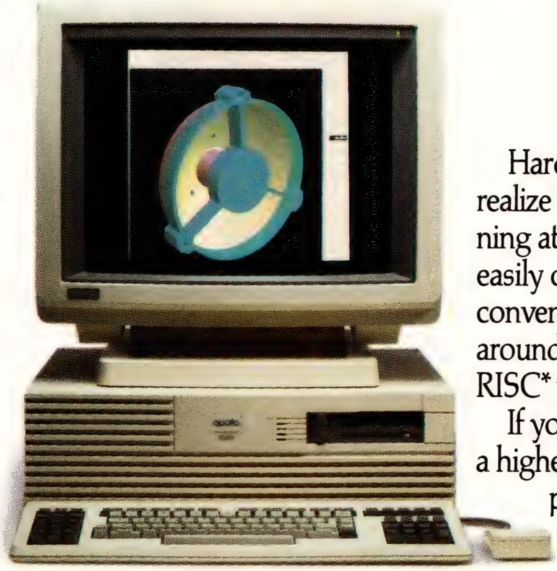
For example, consider two markedly different implementations, one based on Cirrus Logic's GP340, the other based on Weitek's XL-8200. Each printer controller created a bit map for an identical page of text and graphics. The page contained several different type fonts and sizes, and the graphics were merged with the text. Each manufacturer used a stopwatch to measure the time it took for the controller to complete a bit map for that page. The controller using the Cirrus chip took 90 sec to create the page; the board using the Weitek chips created the page in 38.4 sec. The times quoted for each board are for font and bit-map creation only; they don't include the actual printing time, which depends on the print engine.

The application containing the GP340 is a PC/AT-based plug-in board for a dumb print engine. The controller board uses the PC's 12.5-MHz, 1-wait-state 80286 as the processor, because the GP340 is a coprocessor. The board has 2M bytes of 120-nsec dynamic RAM; 1M byte is the image memory (primarily the bit map), and the other 1M byte is devoted to the font cache, display lists, and patterns. The Postscript-compatible interpreter is from MBA Software (Santa Clara, CA) and runs under MS-DOS. Because of MS-DOS's 640k-byte memory limitation, the laser printer's 2M bytes of RAM runs under the Lotus/Intel/Microsoft EMS (Expanded Memory System) for MS-DOS. EMS requires the processor to switch the memory banks in and out of main memory; a system running an operating system that can access at least 2M bytes of memory should run markedly faster. Cirrus estimates that the total cost for the controller, exclusive of the memory, would be between $50 and $75.

In contrast, the controller based on the Weitek XL-8200-40 is a stand-alone board. The "-40" suffix indicates that the chip set can support print engines to about 40 pages/minute; this version of the chip set costs about $199. The board's 3M bytes of RAM are divided into 2M bytes of page-image memory and 1M byte of memory for font and pattern storage. The memory is 120-nsec static-column dynamic RAM. Running in static-column mode requires extra hardware (in this case, it's implemented in erasable programmable logic devices, or EPLDs), which is justified by the speed increase; when accesses are made within the same 256k-byte block, the access time is 60 nsec. Although this board would probably cost about $400 to make, you could build it less expensively by using ROM instead of EPLDs, which are relatively expensive. Note that for both designs, the cost of the control electronics is smaller than the cost of the image memory. Dynamic RAMs currently cost about $200/megabyte.

To see how boards using these recent printer-control ICs measure up to earlier printer-controller implementations, Weitek measured the time it took for an Apple LaserWriter Plus to create the fonts and bit map of the same page of text and graphics. The LaserWriter Plus, a popular laser printer that was designed before these printer-control ICs were available, uses the 68000 with no coprocessor for hardware acceleration. It took 185.5 sec.

APOLLO TURNS 030.



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 CIRCLE NO 104

Printer-control ICs

Neither of those facts represents a drawback, according to Dale Dewoskin, engineering manager at Personal Computer Products. After all, he asserts, lower-resolution, non-Postscript printers, which will continue to carry the majority of the market, spend the greater part of the print cycle in performing CPU processing that's very difficult to accelerate in hardware. At 300-dpi resolutions, BitBlts don't require as much processor time, and low-end systems will not bear a RISC approach such as that used in the Weitek chip set. Dale adds that Postscript engenders a cost/speed tradeoff—the price of any printer that runs Postscript varies directly with the print speed.

PCPI's LPC1 chip includes a CPU interface to the 68000, dynamic-RAM control, and a DMA interface between the bit map and the engine. The chip is tentatively priced at under $15 (OEM qty). PCPI used Motorola as the foundry for the chip, so you can buy the laser-controller chip from Motorola, and you may be able to get both at a lower price. The company plans to release a chip that does incorporate BitBlt functions in mid-1989. The chip, the ALPC-1, will cost less than $30.

Western Digital's WD65C10 page-printer interface controller also implements the CPU interface, the dynamic-RAM control, and the DMA interface, although it's not as processor-specific as the LPC1. The 65C10 allows software-programmable print-engine support, a useful feature if your electronics must support a full line of dissimilar engines at different resolutions. None of the engine-control signals are standardized, and although the video-data signal is standard, virtually none of the other control signals are. For example, if you use a Canon print engine, your control electronics must provide a clock; if you use a Ricoh print engine, which provides a clock, you must make sure your control electronics are in sync with the clock. In the 65C19, these parameters are software selectable. Note that this chip could be used in conjunction with one of the more powerful chips, such as the National Semiconductor 32CG16, which lacks DRAM-control circuitry. The 65C10 costs $11.20 (10,000).

All of the laser-printer-control ICs discussed so far are recently introduced parts intended specifically for the laser-printer market. However, some other recently introduced processors that are not limited to application in laser printers can also make good laser-printer controllers.

You could use the AMD 29000, for example; it's a general-purpose RISC processor that costs $174 to $300, depending on the speed version. The company claims that various third-party Postscript-compatible interpreters for this chip will be available early in 1989.

The TMS34010 graphics processor from Texas Instruments is a general-purpose 32-bit chip with an external 16-bit address bus. The IC doesn't implement BitBlts in hardware, nor does it use RISC technology; however, Texas Instruments claims that the chip performs BitBlts at a speed comparable to the speeds of the Cirrus, National Semiconductor, and Weitek chips. You can use the IC with video RAM or dynamic RAM; it has built-in controllers for both. It's priced at $45 (OEM qty).

In sum, when you're choosing a laser-printer-controller IC, you won't be able to get away with a quick glance at the spec sheets to make your selection; the subject is too complex. Instead, your choice of a laser-printer-controller IC will depend on a variety of factors, such as the printer-control language you'll use and the ratio of text to graphics that your printer will be expected to handle. The most important factor will be the big tradeoff between bit-mapping speed and cost. EDN

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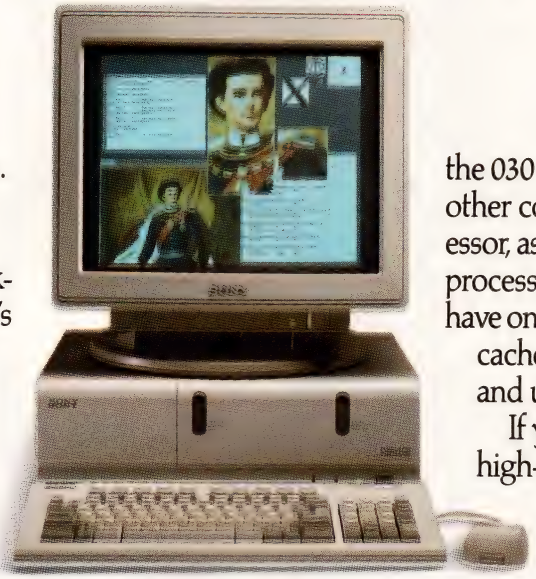

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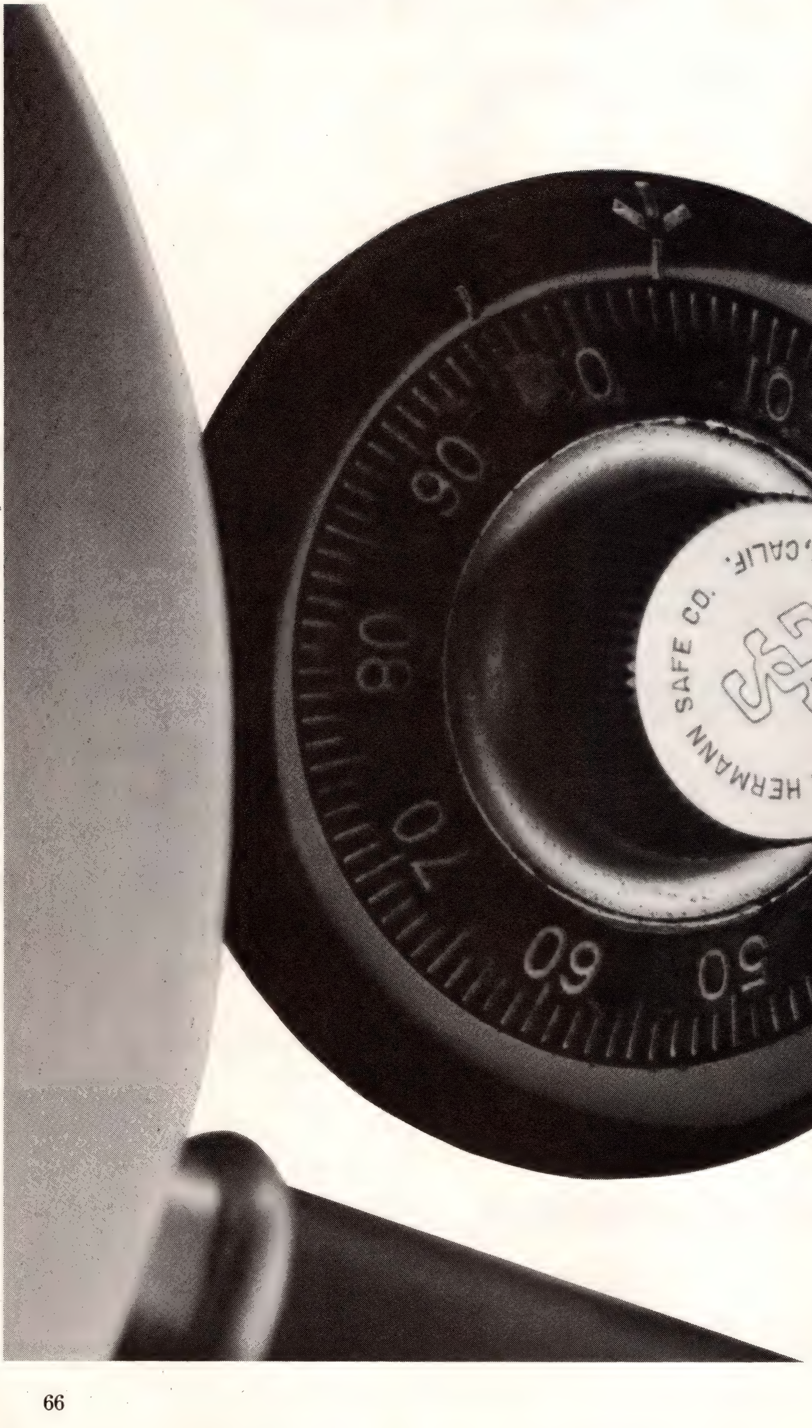

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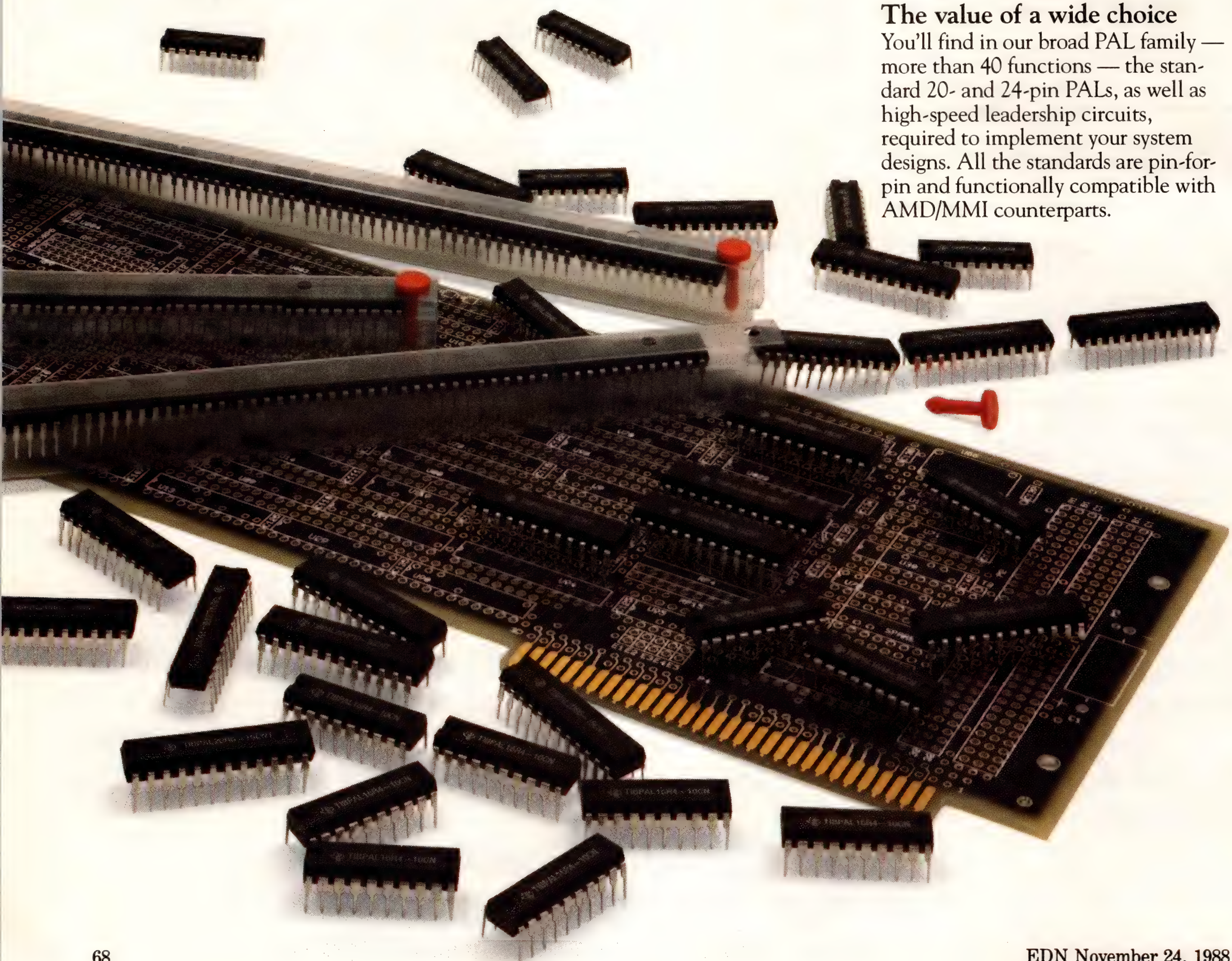

ASIC DESIGN

High-density ICs need design-for-test methods

If you don't consider the testability of your ASIC design from the outset and design features into your circuit that provide for controllability and observability, you may not like what the test and manufacturing departments have to say about you.

Michael C Markowitz,
Associate Editor

To ease the test crunch that ensues from designing 30,000-gate ASICs with less than 200 control or observation points, you need to add new tricks to your design repertoire. Consider the following scenario. After six months of dedicating your life to your ASIC design—conceiving a floorplan, designing the architecture, choosing the logic gates, simulating, evaluating, resimulating, placing gates, routing the interconnections, resimulating again, and running layout checks—you've finally finished your 30,000-gate gate-array design and passed the layout and simulation results along to test and manufacturing. In less than a month, wafers will be out of fabrication and the test engineers will get to plug your ASIC into their fixtures and proclaim you a "Great Designer." If you haven't considered the testability of your design from the beginning and designed features into your circuit that provide for controllability and observability, you may not like what they will call you.

Even though the idea of including performance and real-estate penalties in your design is painful and difficult to accept, the alternative is even more troublesome: An untestable circuit is not suitable for shipment to customers. Until someone develops the capability to reliably test immense circuits in which test considerations have been neglected, ASIC designers will have to keep testing constraints in mind. The question isn't *if* you should consider testability in your design, but *when.*

Partitioning, scan testing, and built-in self-test (BIST) are three of the most popular techniques available to ASIC designers who want to increase the probability of catching device failures. Your selection of the appropriate method depends on circuit complexity, packaging considerations, the application, production volume, fault-tolerance requirements, and chip, board, and system test requirements.

In the past, ad hoc test approaches were acceptable. ASIC designers spent far more time designing than test engineers spent testing, testers were relatively inexpensive, and exhaustive simulations generally yielded reasonable fault coverage at moderate cost.

Two factors have radically changed the cost/benefit equation and have led to a re-examination of the way in which you should design and test your ASIC. First of all, as pin counts have grown arithmetically, gate counts have grown geometrically, and potential internal circuit faults have grown exponentially. Second, typical VLSI circuit testers now fetch better than $1 million. In fact, Jon Turino of Logical Solutions Technology and cochairman of the IEEE P1149 test bus working group, estimates that testing can account for 40 to 50% of total ASIC design costs.

Economic and customer pressures are motivating ASIC vendors to incorporate design for test, or DFT, features into their semicustom libraries. In spite of these pressures, however, some barriers to the widespread adoption of DFT still exist.

Many design engineers, either through inexperience, a failure to quantify the cost of testing, or the

political structure of their organizations, are naive about the impact that testing has on their designs. A number of ASIC vendors, on the other hand, are reluctant to address testability for another reason. In the absence of industry-wide standards, they fear that their individual solutions will have limited acceptance and that they will not be able to recover development costs.

The costs associated with designing for test are difficult to quantify. One of the costs you should consider when weighing DFT is the additional time the project will require during the design phase. You, as the design engineer, must assume much of the responsibility for testing your device even as you define the operation of that device. To make an informed decision, you need to learn more about the total costs of ownership: How expensive is a designer's and a test engineer's time? What is the cost of the design and test hardware? What costs can you pass on to the customer in development? In production? Only after you understand what the true costs of testability are, can you realistically evaluate the tradeoffs between IC real estate, performance, power consumption, pin count, and ease of test.

Try partitioning

Partitioning your ASIC into smaller pieces and multiplexing the control or observation points—I/O—increases both controllability and observability (the ability of either you or the test equipment to view the value of a particular node embedded within a circuit). The cost of test-pattern generation is roughly proportional to the number of gates cubed; by dividing a circuit in half, you can realize an 8:1 savings in test costs.

You can, of course, design testability into your circuit independent of your ASIC vendor. As an alternative, however, a number of vendors have incorporated features into their macrocell libraries that transform testability into a drop-in component. If you use these macrocells and provide access to all of the macrocell's I/O, the ASIC vendor can test the cells irrespective of the rest of the IC's logic. It may be helpful to think of this methodology as allowing you to "probe" the macrocell at the chip level. The vendor will often have a pre-existing test program to test the macrocell; you then have to write a separate test program to test just the random logic.

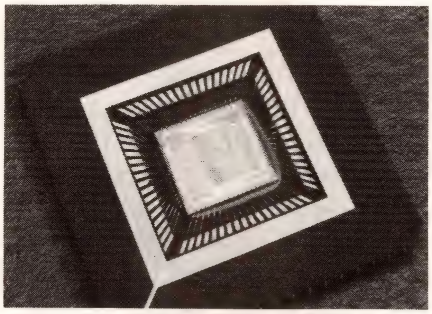

***Fig 1—You can surround** this standard-cell 16-bit microcontroller core of a macrocell with multiplexers to permit access to its I/O. National Semiconductor's HPCCOREA offers 64k bytes of external memory addressing, a 135-nsec cycle time (when using a 30-MHz clock), and high code efficiency because instructions are mostly single bytes.*

National Semiconductor's HPCCOREA is a good example of such a macrocell (**Fig 1**). The vendor's suggested test strategy is for you to surround the core with multiplexers to isolate the cell from the remainder of the ASIC logic, which allows them to guarantee the function of the core in the ASIC design. By using the core as a controller, National Semiconductor follows up the core test with a separate test of the IC's surrounding peripherals and glue logic.

In its cell library, Sierra Semiconductor includes the COP800 microcontroller, which has four modes of operation. In the normal mode, the core executes your application code from internal ROM or EEPROM. While the core is in its ROMless mode, you can develop or debug code executed from an external PROM or EPROM under the control of the company's emulator. When the microcontroller is in the core-test mode, you isolate and test only the core; when it is in the peripheral mode, you use the core to test the "noncore" logic.

Intel has adopted a similar technique for some of the macrocells in its ASIC libraries. For the UC51xx and UC52xx 8-bit microcontroller families (which differ only in the relative allocations of ROM and RAM), Intel has built an isolation ring around the core. The company uses the isolation ring to make the core compatible with its standard cell system, to simplify testing, and to keep pin-count overhead down to four additional pins. By forcing the chip into a particular test mode, the isolation ring directs certain core signals to the ASIC's I/O pins. After the core has passed functional testing, you can use it to generate signals for testing the peripheral logic.

Harris's RTX processor, a RISC processor that executes a Forth-language virtual machine in hardware, is slightly different. This cell is available as part of Harris's ASIC library, but the vendor can test the core processor independent of the associated circuitry only if you provide all the RTX I/O at the chip's periphery.

Scan testing: an alternative

Circuit partitioning is not a highly structured DFT technique, and in some applications, a somewhat more structured method may be appropriate. Scan testing allows you to configure your sequential logic into a shift-register chain so that you can test your ASIC as a combinatorial circuit. There are many variants to scan testing.

ASIC design

Among the most popular are IBM's Level Sensitive Scan Design (LSSD), Nippon Electric's Scan Path, Sperry's Scan Set, Fujitsu/Amdahl's Random Access Scan, and Honeywell's Synchronous Scan Design (SSD). Although each implementation of scan testing offers its own clocking, data-latching, or data-accessing scheme, the underlying theory is basically the same.

A simple analogy of scan testing and a roadway will suffice to illustrate the concept. Cars entering a roadway from side streets are occasionally stopped at traffic signals. Think of the road as the combinatorial logic, the traffic lights as the flip-flops, and the cars as the signals propagating through the logic. The flip-flops' Q outputs provide the circuit with observability; either the scan clock or the system clock updates the outputs (the traffic light turns green, letting the cars through the intersection). The D inputs to the flip-flops give controllability to the combinatorial logic preceding the flip-flops (the traffic light turns red, stopping the cars).

As a simple practical example, consider the circuit in **Fig 2.** Each scannable flip-flop has two clock inputs: C, the system-clock input, and SC, the scan-clock input. Of the two data inputs, D comes from the output of the combinatorial logic, and SI results from the preceding flip-flop in the shift-register chain.

First, you test the flip-flops by shifting data through the chain by toggling the SC clock. After verifying the operation of the registers, serially preload the registers through the scan input. After the shift register is properly loaded, the tester toggles C once to allow the data to flow through the combinatorial logic. The tester toggles SC to shift out the combinatorial result. You can repeat this procedure until you've evaluated all potential stuck-at faults.

All the access you want

The advantage to configuring your latches and flip-flops into a shift register is that you have access to all inputs and outputs through two pins. Automatic test generation (ATG) programs, such as Gateway Design Automation's Testscan, Aida Corp's (a Teradyne EDA subsidiary) Aida ATPG, and Silicon Compiler Systems' ATG, can generate vectors to test the combinatorial logic between latches. These programs typically achieve fault coverage of almost 100% as long as the

Fault coverage can provide a clue

Fault coverage is a way to measure the effectiveness of a test program. The fault model is based on the "stuck-at" model, which assumes that signal lines can be shorted to ground (stuck at zero) or shorted to the positive supply (stuck at one). You can extend the model to apply to any condition that causes a gate to behave as though one of its nodes is stuck at one or zero. According to Prabhu Goel, president of Gateway Design Automation Corp, "The fault model is *only* a model of mechanical failure; nevertheless, history has demonstrated that an excellent correlation exists between the model and actual design faults."

The model can account for defects such as open interconnections, shorts between conductors, excess leakage current, electromigration, and overload-induced burnout. Although multiple faults can occur, the model simplifies the analysis by considering only single faults.

Typical functional test patterns exercise an IC and show 60 to 80% fault coverage; even though every node may be toggled, a node may have no observability when it is exercised. You could argue that if you present all possible functional inputs to your ASIC, then the fault coverage shouldn't be important. Goel counters that unless the circuit is strictly combinatorial or a very simple sequential circuit, there is no way to ensure that every possible functional pattern is applied to every state of the circuit.

As further evidence of the efficacy of the fault-coverage model, a joint study by Motorola and Delco found that 50% fault coverage yielded a 7% defect rate (7 bad parts per 100 tested "good") and 90% fault coverage uncovered a 3% defect rate **(Ref 1).** To generate a 0.01% defect rate, the study found that it would be necessary to test a circuit for 99.9% fault coverage.

Applying functional patterns quickly reaches a point of diminishing returns; each subsequent pattern detects fewer faults. The most economical way to achieve high fault coverage is by using DFT techniques and nonfunctional test patterns.

Reference

1. "Logic Fault Verification of LSI: How It Benefits the User," Harrison, R A, R W Holzwarth, P R Moltz, R G Daniels, J S Thomas, and W H Wiesmann, *Proceedings of the WESCON Professional Program,* September 1980.

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designs they examine don't have any redundant circuitry.

Integrated Logic Systems (ILS), a small CMOS ASIC company, takes an integrated approach to testability that combines its scan-testable architecture with ATG software to automatically generate high fault coverage (see **box**, "Fault coverage can provide a clue"). ILS combines ROM, RAM, PLA, and macrocells on an array that alternates rows of scannable sequential logic and combinatorial logic. A special power grid minimizes noise effects on the array.

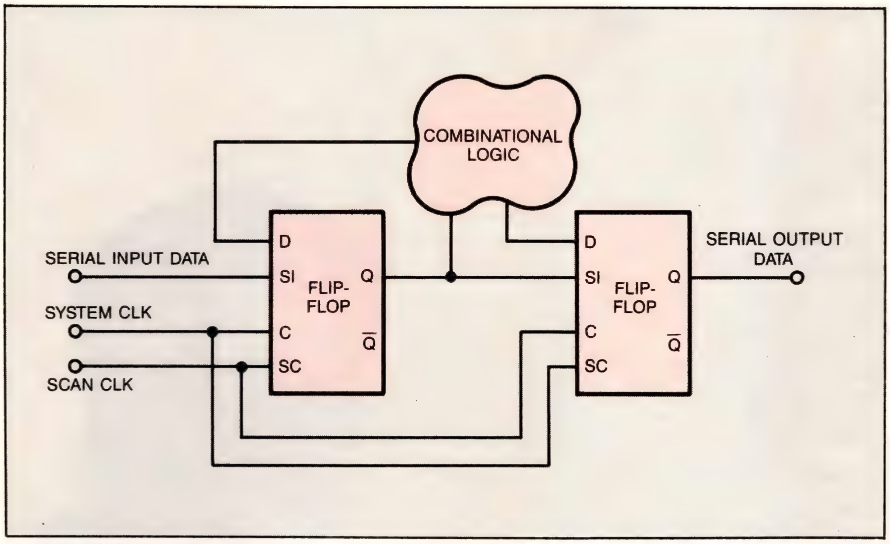

***Fig 2—In a typical scan approach,** you serially shift the data through the registers to preload them. The tester then toggles the system clock once to exercise the combinatorial logic and serially shift out the result.*

Unfortunately, scan testing incurs overhead costs—greater flip-flop size and slower circuit speed—that may have a negative effect on your design. The impact, both in performance and real estate, depends on the scan methodology and what percentage of your design is register based. You must weigh these costs against the savings you'd realize from a shorter test cycle. You should be aware that you may be able to accrue cost benefits by using a new type of IC tester, which is significantly less expensive than typical VLSI circuit testers (see **box,** "A new and different tester makes its debut").

Because it is convenient to test an ASIC as if it were a pc board, you might want to implement a functional test pattern to verify the operation of the macrocells embedded in your design. Texas Instruments takes this approach to DFT. PMT (parallel module testing) is most useful for cells that have a pre-existing test pattern. It involves

A new and different tester makes its debut

Can you imagine a VLSI tester that costs less than \$2000/pin—when typical testers cost \$5000 to \$10,000 per pin? According to Tom Huang, founder and president of Gillytron Inc, the Scanmaster GT-8005 costs just that and sacrifices only some flexibility. Although you can't run typical functional test patterns whereby you drive all the inputs and monitor all the outputs, if you've implemented a scannable design, you may be able to do the tests you need and still save some money.

You can expand the 128-pin production scan tester to 1792 pins with the addition of 128-pin function modules. The complete tester consists of an IBM PC/AT-based user console, a scan module, a control module, and the function modules. The scan module incorporates a scan generator that has an interface for 23 clock/control lines, scan-in and scan-out data lines, and power and ground. If your circuit uses IBM's Level Sensitive Scan Design (LSSD), or only transparent scannable latches, or if it has a separate, definable-length scan string of transparent scannable latches or inverters, you can use the scan module to perform a scan-string ac performance test. Holding test and clock lines at the proper dc levels and closing the loop between scan in and out, the Scanmaster allows the circuit to oscillate at its natural frequency, based on the scan path length. The tester can measure ring frequencies of 2 kHz to 100 MHz to 0.1% accuracy.

The scan module's pattern memory is 4M bytes (expandable to 256M bytes). As many as four scan generators can fit in a scan module—one is standard—and the tester can accommodate either one or two scan modules. A programmable power supply in the scan module forces either current or voltage for dc parametric tests.

A 128-pin Scanmaster GT-8005 starts at \$240,000. Additional functional modules, each of which add 128 pins of capacity, cost \$90,000 apiece.

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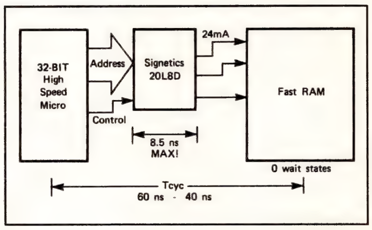

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"addressing" a macrocell in an ASIC, applying input patterns to all of the cell's inputs, and verifying the cell's responses at the outputs. The technique requires that you interface the test I/O through 3-state buffers controlled by a test pin.

A TI software program, Detector (which also performs design rule checking), provides verification that you have correctly implemented the PMT testability logic. Pin overhead for PMT may be as little as two pins if your ASIC has more I/O than any of the macrocells (to allow for access to all of the signals).

LSI Logic offers a fully scannable MIL-STD microprocessor core, the 1750A, but if you feel that your design can't afford the performance and I/O penalties of a scan design, you can test the core by multiplexing the cell I/O to the periphery (**Fig 3**). Because the core cell in LSI Logic's 1.5-μm technology is 350 mils², the company estimates that you can add an extra 20,000 to 25,000 gates of circuitry.

Fig 3—With this microprocessor core, *you have a choice of two versions. You can either provide for scan testing of the LSI Logic 1750A core or you can multiplex out the I/O.*

The IEEE to the rescue

Because many of the DFT and scan-testing techniques being developed independently are largely incompatible, the IEEE is working on a standardized test bus in an effort to bring order out of chaos. Designated P1149, the bus has four subsets. P1149.1 is the Minimum Serial Digital Subset, which defines boundary scanning and the on-chip ports to BIST. P1149.2 is the Extended Serial Digital Subset, which defines implementations of scan testing like LSSD and Scan Path. P1149.3 is the Real Time Digital Subset, which can use both structured and unstructured techniques. And P1149.4 is the Real Time Analog Subset.

At the International Test Conference in Washington, DC, during the week of September 12, the P1149 working group reached an agreement with the Joint Test Action Group (JTAG) that provides for JTAG's development of its own documents and protocols for the Test Access Port (TAP) under IEEE P1149.1.

JTAG is an industry-wide organization with the mandate to establish a standard test methodology. Systems companies initiated the concept of a standard test methodology because they wanted to eliminate the problems that would result from each vendor creating components that might be independently testable but whose test strategies would be incompatible in a system.

The organization is devoting its efforts to building a framework within which you would have access to and control of built-in test facilities of components and which would also give you the ability to convey test data to or from the boundaries of individual components. At present, the framework centers on boundary scanning, a technique using scan-testing principles that involves the inclusion of a shift-register latch adjacent to each component pin to allow controllability and observability of the periphery of an IC, coupled with a test access bus. The JTAG V2.0 overhead is four pins: serial data in, serial data out, clock, and control. For a minimal implementation in a 36-mm² IC built with a 2.0-μm CMOS process, boundary scanning exacts about a 3% area overhead.

Philips Components was the driving force behind JTAG's formation. The manufacturer embraced, refined, and extended boundary scanning from the system level down

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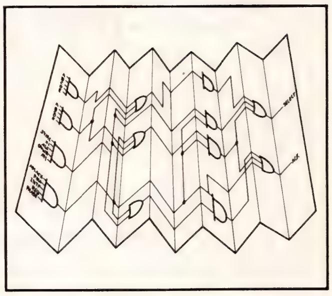

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to the component level. Philips' approach conceptually equates pc boards with ICs and ASICs with macrocells.

If you adhere to Philips' design methodology, when the chip enters the test mode, the vendor uses internal scan techniques to "address" and test each of the macrocells in your circuit. The test program then evaluates the combinatorial logic outside the macrocells, again using internal scanning. Finally, the program verifies interconnections between macrocells using a boundary-scan-like approach. The cost of adopting this technique is less than 20% of the circuit area and between 3 and 10 pins, depending on the complexity of your design and the quantity and parallelism of the test logic you require.

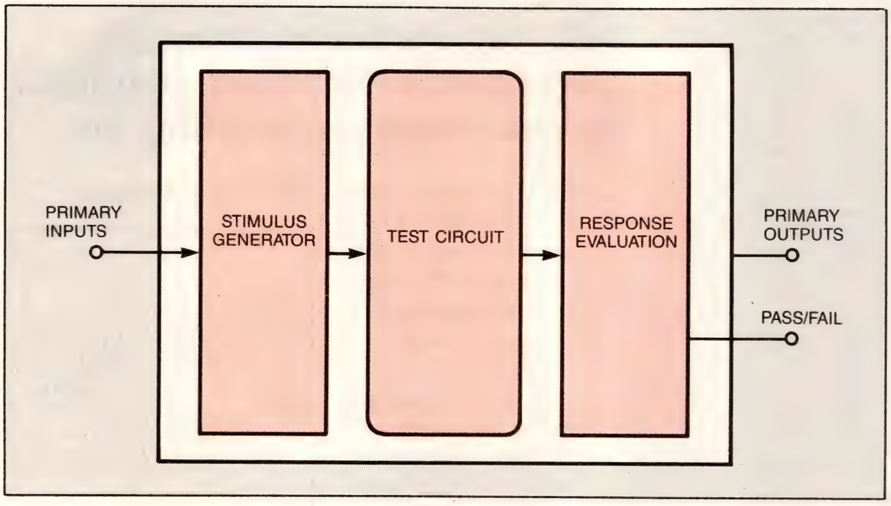

***Fig 4—In a self-testing ASIC,** the primary inputs seed the stimulus generator to exercise the circuit. A signature analyzer or set of comparators then evaluates the response against the expected result.*

Self-test is on the rise

As the testability issue has become more important, designing ASICs with the capability to test themselves has gained in popularity. **Fig 4** illustrates the concept of self-testing circuits. BIST achieves dramatic savings in the cost of test-

For more information . . .

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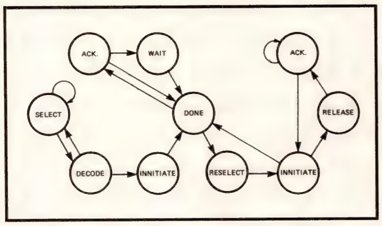
Clak! At last, advanced state machine design is easy. Signetics Programmable Logic Sequencers (PLSs), including the new 50MHz PLUS405, have a unique architecture that employs buried registers to store intermediate values. The result—greater silicon and pin utilization with increased system functionality.



Advanced state machine designs become easy with Signetics sequencers.

Clak! IF-THEN-ELSE functionality. Signetics unique architecture makes complex IF-THEN-ELSE states possible. Connecting any AND term to any OR term (product term sharing) eliminates redundant state transition terms. And JK or SR type registers optimize the logic used in generating state transitions.

In addition, all our PLDs are supported by ABEL, CUPL or our powerful AMAZE software with auto test vector generation to make your job easier.

Clak! We've got the guts! That's right, we have those essential PLDs you need to improve total system performance. PAL®-type devices, Programmable Macro Logic, Logic Arrays and our high-speed PLSs with buried registers that make advanced state machine design easier.

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ing by reducing (or eliminating) test pattern generation, shortening the test time by running tests at circuit speed, and reducing the requirements for external test equipment.

Different vendors have different approaches to self-test. ETA Systems calls its approach BEST (built-in evaluation and self test), for instance. Control Data Corp uses two techniques: OCMS (on chip maintenance system) and VISTA (VLSI integrated self-test architecture). Although each method has certain characteristics that differentiate one from the other, the basics of self-test are the same. They usually use linear-feedback shift registers (LFSRs) to generate pseudorandom sequences of data to drive a circuit and use other LFSRs to compress the test results. Logic in the ASIC or in the tester compares the compressed results, or signature, against a known-good signature to validate fault-free operation.

Use LFSRs to test RAM

To test RAM embedded in an ASIC, AT&T uses a parametric, modular approach customized to the organization of the RAM. The test program reconfigures the address latch and read/write registers to function as a counter, and two LFSRs then generate input data and read/write patterns and use the counter outputs to generate their inputs to the static RAM. Internal logic compares the memory against the results expected from a data generator; the results of the comparison are compressed to a 1-bit BIST flag. As a final check, the LFSRs verify the operation of the self-test circuitry. The overhead is four input and two output pins, and, for a 4k-byte static RAM about 13% more area (**Fig 5**).

With the HC Series of gate arrays from Honeywell, you get the ability to field test your ASICs at a cost of four pins—TCE (test clock

TABLE 1—COMPARISON OF DESIGN-FOR-TEST TECHNIQUES

TECHNIQUE	ADVANTAGES	DISADVANTAGES	OVERHEAD	COMMENTS
PARTITIONING	• LOWEST CIRCUIT OVERHEAD • MINIMAL PERFORMANCE IMPACT	• MANUAL PATTERN GENERATION • NO GUARANTEE OF FAULT COVERAGE • MAY NOT APPRECIABLY SIMPLIFY TESTABILITY	<5%	• HAS LOWEST IMPACT ON CIRCUIT SIZE AND PERFORMANCE; MAY ALSO HAVE LOW IMPACT ON TESTABILITY. • GOOD FOR STRUCTURED DESIGNS
SCAN TEST	• COMPUTER-GENERATED PATTERNS • HIGH FAULT COVERAGE • HIGHLY STRUCTURED APPROACH FORCES MANY GOOD DESIGN PRACTICES	• REGISTERS BECOME LARGER • ADDITIONAL CONTROL LINES MUST BE ROUTED TO REGISTERS • TEST IS PRIMARILY SERIAL; GENERALLY LONGER THAN FUNCTIONAL PATTERNS. CAN RUN PARALLEL PATHS	10 TO 20%	• NUMEROUS VARIATIONS (EG, LSSD, SCAN PATH, SERIAL SCAN TEST)
BUILT-IN SELF-TEST	• EXECUTES AT CIRCUIT SPEED • CAN REDUCE PRODUCTION TEST COSTS • CAN BE USED IN FIELD TEST AND DIAGNOSIS	• REQUIRES SCAN-TEST FOUNDATION • REQUIRES CONTROL CIRCUITRY AND LFSRs FOR PSEUDO-RANDOM PATTERN GENERATION AND SIGNATURE ANALYSIS	SCAN + ~2%	• OFFERS GREATEST POTENTIAL FOR MINIMIZING TEST COSTS

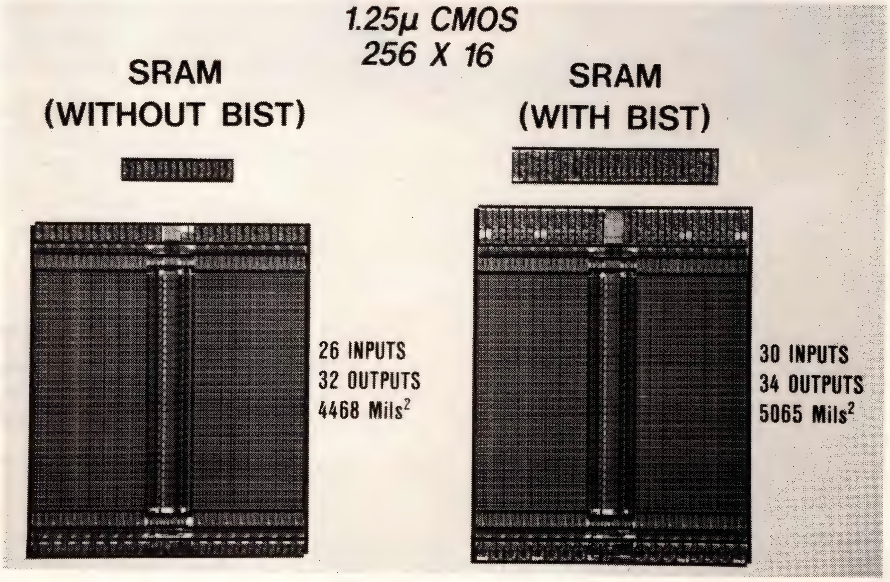

Fig 5—If you implement a static RAM with BIST, *you'll only pay a 13% area and 6-pin penalty, yet you'll still simplify your test task (photo courtesy of AT&T).*

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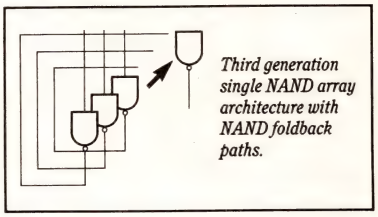
Click! A programmable "instant" gate array. The PLHS501, the first of our Programmable Macro Logic (PML) products, provides up to 1300 equivalent gates—a complete solution in a 52-pin PLCC package. And its wide NAND input capability makes it ideal for high-speed address decoding and bus interface applications.



It's also the easiest way to reduce your NRE costs, inventory problems and quality concerns. It's easy to use because it's supported by our powerful AMAZE software which gives you a complete system in an instant.

Click! AND/OR design constraints vanish in an instant. Signetics folded NAND array architecture provides 100% interconnectibility to eliminate routing restrictions. And 100% gate selectability to build flip-flops, multiplexers and decoders resulting in total silicon utilization.

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enable), TDI (test data in), TDO (test data out), and TST (test strobe). To begin the test, you load a control word into the BEST (licensed from ETA Systems) control-word register and a seed word into the input register. By manipulating the TST and TCE signals, you can stimulate the array and generate outputs that are stored in the BEST output register. The tester shifts the checksum value off the chip and verifies it to determine chip integrity.

To further address DFT, Honeywell also includes scan-testable latches and flip-flops in its libraries so you can have two mechanisms for detecting design or manufacturing faults. Honeywell has also demonstrated its commitment to DFT by offering DFT training courses to companies and engineers who wish to use its libraries to design and build ASICs.

Honeywell isn't the only ASIC vendor that's invested heavily in DFT. Different vendors have different approaches, however, and the particular technique that you should use is highly dependent on your circuit and its application. All of the suggested DFT techniques require that you make difficult decisions: No one technique is appropriate for all circumstances. You do, however, have to be aware of the issues, concerns, and tradeoffs involved in using partitioning, scan-test, and BIST techniques before you can make an intelligent decision. **Table 1** may be helpful in this regard. EDN

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PLESSEY KEY PROCESS TECHNOLOGY

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DESCRIPTION	F_t	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	400MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μm	3-5V
MH/MA SiGate CMOS	30MHz	4μm	3-15V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

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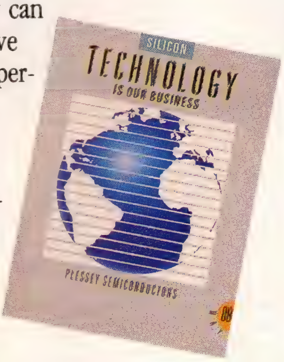

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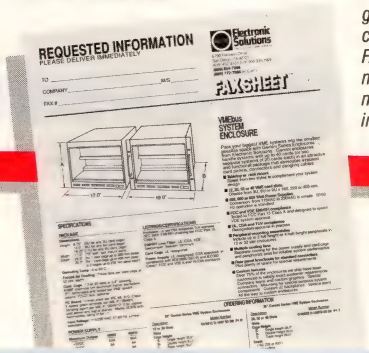

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C compiler for microprogramming optimizes custom architectures

Using a standard high-level language to microprogram custom architectures may seem like a contradiction in terms, but not any longer. The MetaStep C compiler allows you to do exactly that.

You begin by defining your architecture with a series of machine-definition statements. These statements allow you to specify the instruction length, bit and field definitions, macroinstructions, and symbolic values. You can even create case definitions, defining fields that vary in meaning for different instructions. The macroinstructions and values, once defined, are available to the entire language system, allowing you to use them in your application program.

You can also use the machine definition to relieve the burden of remembering the programming constraints of your system. You can specify which values are legal for the various fields and which values are valid in context with other fields—for example, you can specify that an instruction cannot direct two different resources to access the same bus simultaneously. The compiler will then identify and flag any violation made by your application program.

Once the machine definition is completed, you may begin your application programming. The compiler will accept any combination of C, assembly, and bit-vector-level statements. The lower level statements have a freeform, position-independent syntax and will accept both absolute and symbolic values.

As it processes your program, the compiler's front end performs a number of machine-independent optimizations. These include live/dead analysis, recognition of reused expressions in the body of your code, and the elimination of common subexpressions. The compiler's back end performs machine-dependent optimization on your program, using the machine definition you specified. It then assembles and links the final code.

Because the files generated by the various parts of the compiler are on a common database, you can pass the language constructs to your debug tools. This procedure lets you debug your code at the source level, using the same symbols that are in the program definition. Included in the output files are binary and hexadecimal code files, a symbol file with global labels and addresses, and a debug file.

The software is available for both single-user and multiuser environments under MS-DOS and Unix. The single-user version for MS-DOS costs $4995. The version for Sun workstations running Unix and the multiuser version for VAX/Unix configurations start at $9995 and $19,995, respectively.

—Richard A Quinnell

Step Engineering, Box 3166, Sunnyvale, CA, 94088. Phone (800) 538-1750; in CA, (408) 733-7837. TWX 910-339-9506.

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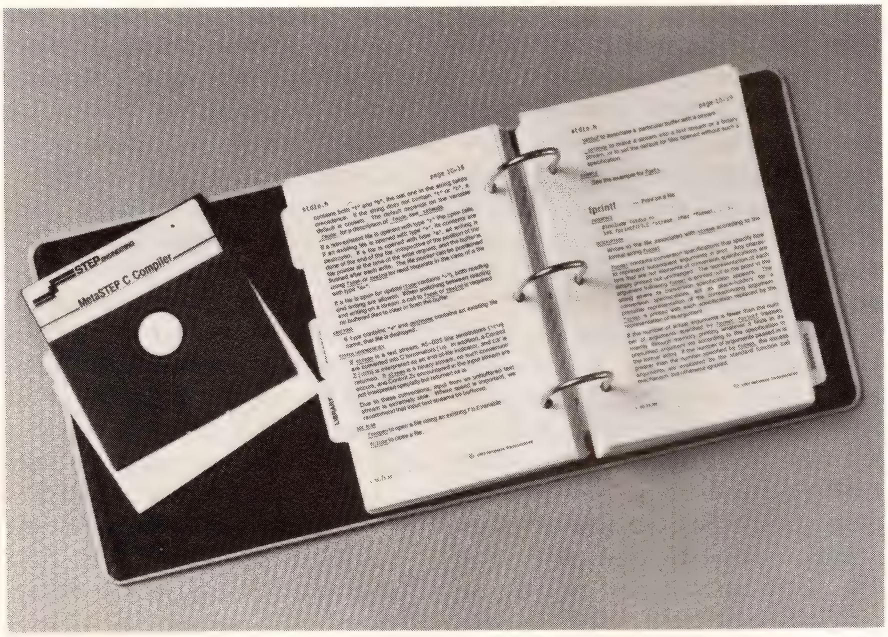


***The Metastep Microprogram C Compiler lets you** write system and application programs in high-level C language for custom microprogram-based systems.*

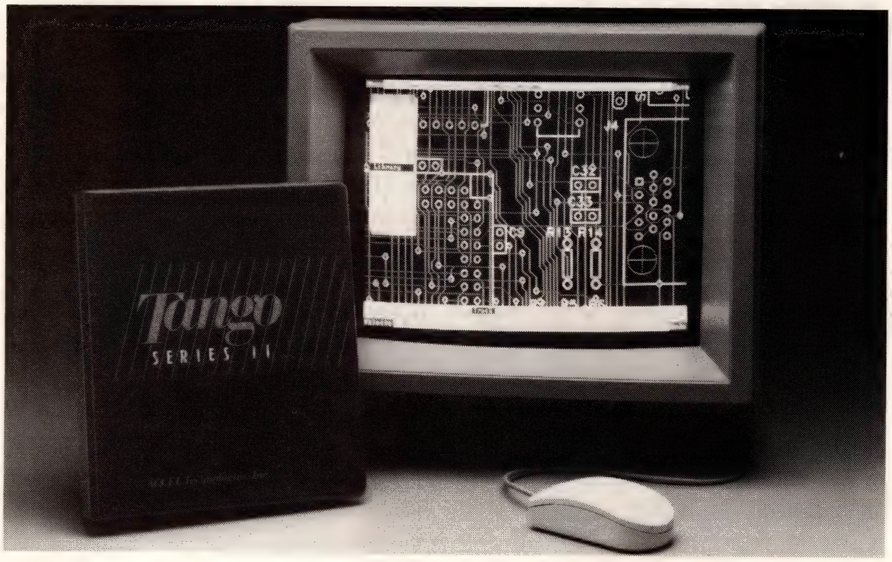
IBM PC-based pc-board design software employs a pop-up menu user interface

The Series II versions of Tango-PCB and Tango-Route pc-board design software employ a user interface based on pop-up menus and dialog boxes, and offer context-sensitive help information. You can use the software to design pc boards as large as 32×32 in., using as many as six signal layers. The IBM PC-compatible software can drive most popular monitors and hardcopy graphics devices.

Though the software is labeled Series II, the Tango-PCB and Tango-Route packages have been developed from scratch, sharing only a name with the original Tango pc-board design software. The new software employs a "fourth-generation" user interface called API (Accel Productivity Interface). The API uses pop-up menus and dialog boxes, but the menus are never more than two levels deep. You can access frequently used commands with a single mouse click from the Speed Palette, which is available for displaying at the bottom of the screen when you choose to do so.

Furthermore, the API screen includes four Hot Spots, one in each corner of the screen. The Hot Spots let you access the main menu, the zoom window, and the Speed Palette, and let you undo commands with a single mouse click. You can also map a number of commands to a keystroke sequence, using the macro feature. A prompt line displays a short description of each menu item or command as you use the API.

You can also design complex pc boards with the personal-computer-based products. The Tango-PCB pc-board layout package supports six signal layers, power and ground layers, keepout and board-outline layers, a connections layer, a title layer, drill-drawing layers, top and bottom silkscreen layers, an assembly layer, and solder mask layers.



Support for 32×32-in. boards with as many as six signal layers *makes the personal-computer-based Series II Tango-PCB and Tango-Route packages competitive with many workstation-based products.*

The pc-board design package offers 1-mil resolution and three grids (snap, visible, and relative) with user-definable increments from 1 to 1000 mils. You can define track sizes from 1 to 255 mil and pad sizes from 4 to 1024 mils, using multiple shapes. You can overlap components with support for double-sided surface-mount technology. And the program provides input, optimization, reroute, and verification support for a net list.

The Tango-Route autorouter employs multipass, maze, and proprietary routing strategies to handle 4-layer boards. The router employs a 25-mil grid, but you can define track and pad sizes. And you can employ multiple track widths by assigning widths to particular nets. The software can perform pad to pad, track to track, track to pad, and electrical design-rule checks on pc-board designs with six signal layers, and power and ground layers.

Both Series II packages support Hercules-, CGA-, MCGA-, EGA-, and VGA-compatible graphics adapters and monitors. The software can drive Hewlett-Packard, Houston Instrument, Roland, and Calcomp plotters; and graphics printers from Epson and Hewlett-Packard. Furthermore, you can use the software with Gerber photo plotters and Excellon N/C drills.

The Tango-PCB package costs $595, and the Tango-Route autorouter sells for $495. You can purchase the packages bundled for $995, including a year of free updates. Owners of the original Tango software can purchase updates for $50 per product. You can expect a Series II schematic-capture program in the first quarter of 1989.

—Maury Wright

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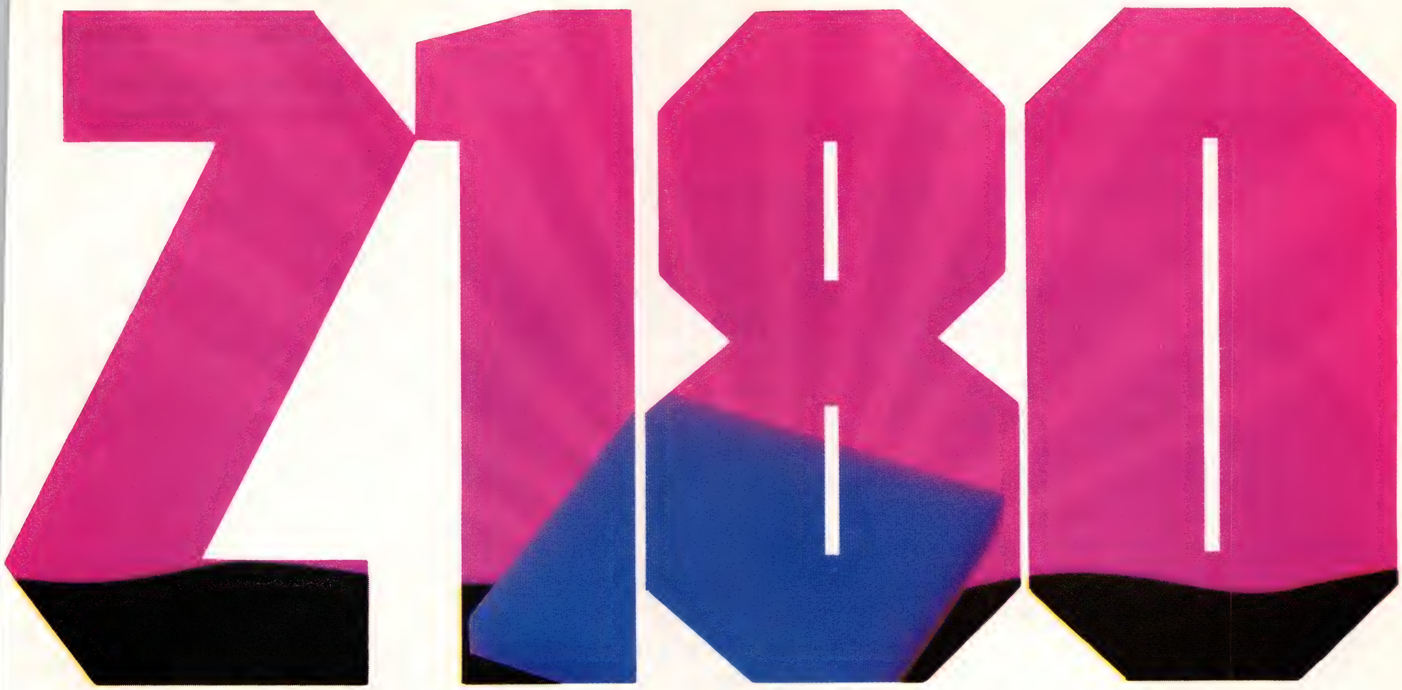

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You'll be up and running with the Z180 immediately. Because it's 100% object code compatible with Z80/8080.™ You probably already know the code, so you can port right onto the Z180. Not only that, since Zilog originally developed the part jointly with Hitachi, the Z180 is directly compatible with Hitachi's version, the HD64180Z.™

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Fiber-optic sensors bring a PC's power to the factory

FiberPak is a fiber-optic-based sensor system designed for equipment manufacturers who use μP-based control systems in their material handling and packaging equipment. The modular sensors are packaged in a case that is plug compatible with single-channel I/O modules that interface with standard computer-bus mounting racks. Sensing options include four modes: through-beam, proximity, true reflex, and polarized reflex.

The system's plastic fibers extend as far as 75 feet and allow FiberPak to interface with a number of the manufacturer's accessories. Lenses are available in a variety of shapes and sizes to increase the sensing range in the through-beam mode. Flexible fiber-optic tips allow the sensors to accommodate proximity-sensing applications in confined spaces. A reflex lens and a polarized reflex lens simplify alignment and reduce interference from reflections. These accessories allow the FiberPak modules to operate anywhere a standard photoelectric control can be used.

In addition to providing a convenient package for OEMs already using panel-mounted I/O racks, FiberPak features improved sensing speed and noise immunity when compared to traditional photoelectric controls. Three FiberPak models are available: a high-sensitivity model with a 15-msec response time; a standard version, which has a 1-msec response time; and a high-speed version with a 100-μsec response time. Over a 6-ft length of fiber, appropriate lenses extend sensing capabilities in the through-beam units to 160, 46, and 16 ft, respectively.

Because all three models operate from 4.75 to 30V dc supplies, you can use a single module in either 5, 15, or 24V systems. FiberPak modules have a 3-year warranty against mechanical and electrical defects and are priced at $90 each.—***Tom Ormond***

Opcon Inc, 720 80th St SW, Everett, WA 98203. Phone (206) 353-0900.

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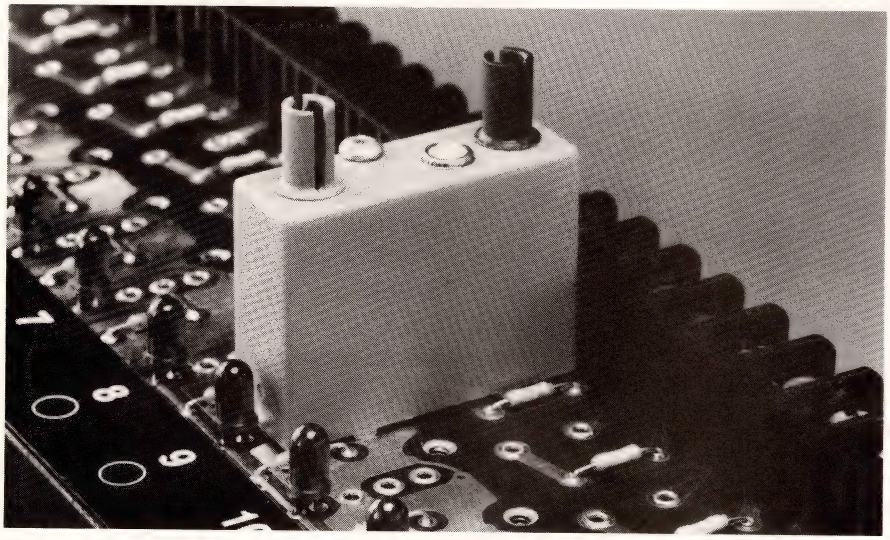

Designed to bring the power of the PC to the manufacturing floor, *FiberPak fiber-optic sensors are available in high-speed and high-sensitivity versions that sense over 75-ft distances.*

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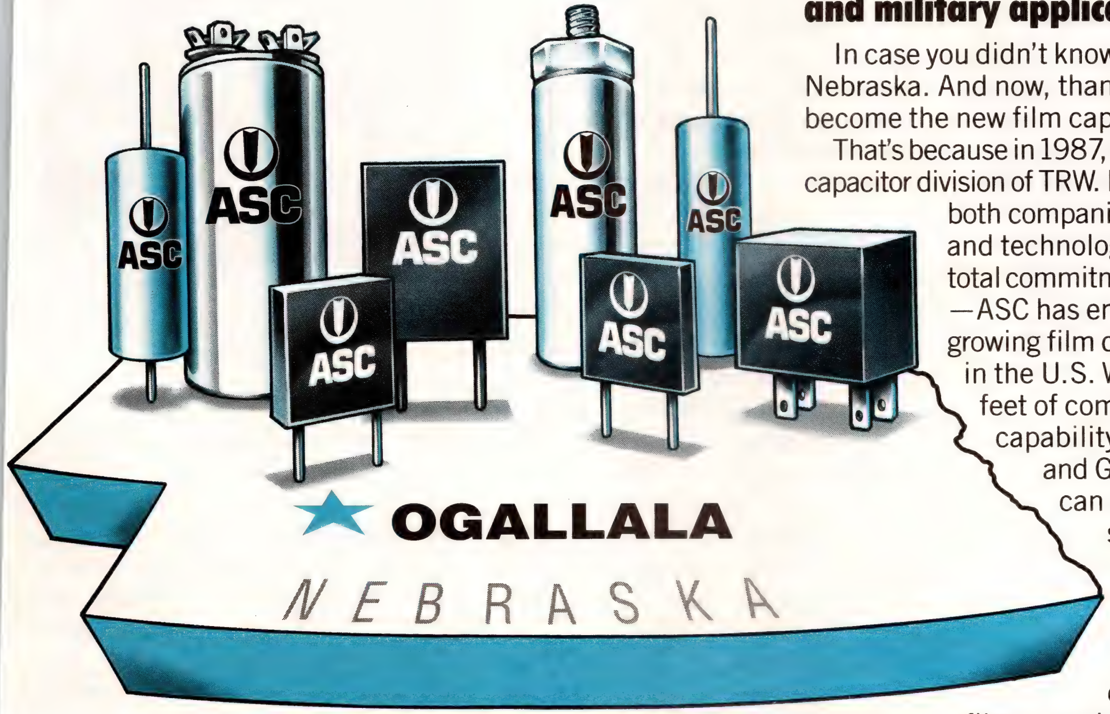

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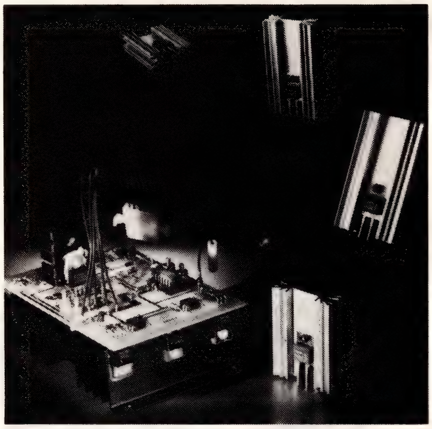
Surface-sensing thermostat controls power supplies

Developed primarily for thermal management of power supplies, the Series 6700 surface-sensing bimetallic thermostat is housed in a TO-220 package that can mount directly on a heat sink. The device is also suitable for use on crowded pc boards or in other temperature-controlled applications where space is at a premium.

The unit features a completely redesigned bimetallic disk, which is rated for a 100,000-cycle lifetime at 5V dc at 20 mA; the mechanical life exceeds 10^6 operations. Gold-plated silver crossbar contacts are standard in both the normally open (close on rising temperatures) and normally closed (open on rising temperatures) versions. The contacts are rated for 1A (resistive) at 48V dc. The contact resistance equals 50 mΩ max before and after life. The operating sense range extends from 40 to 120°C in 5°C increments.

The thermostat's nickel-plated copper mounting bracket, which is isolated from the operating contacts, lets you connect the Series 6700 thermostat directly to a heat sink. The thermostat's surface-sensing ability can detect any over-temperature condition generated by other components that are either mounted directly on, or close to, the heat sink. You can configure the thermostat to turn on a visual or audible signal, switch on or change the speed of a fan, or completely shut down the system when it detects an over-temperature condition.

The Series 6700 thermostat dimensionally conforms to the international Y220/TO-220 product package standard, making it compatible with automatic placement equipment. Using high-speed equipment, you can also solder them onto pc boards. This capability eliminates the need for the expensive hand placement and termination assembly processes typically required for most of today's power-supply thermostats. The thermostat is shipped in a plastic tube that's compatible with automatic-placement equipment and sells for $5.



***Featuring a ±5°C trip accuracy** over an operating range of 40 to 120°C, the Series 6700 thermostat is housed in a TO-220 package that can be mounted directly on a heat sink.*

—***Tom Ormond***

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Dynamic Range	96dB	96dB	96dB	108dB	90dB
Total Harmonic Distortion + Noise	−94dB	−92dB	−92dB	−100dB	−88dB
Conversion/Settling Time	350ns (I_{OUT}) 3μs (V_{OUT})	350ns (I_{OUT}) 3μs (V_{OUT})	350ns (I_{OUT}) 1.5μs (V_{OUT})	200ns (I_{OUT})	4μs
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Portable thermal imaging system costs less than $18,000

The $17,500 Compix 6000 thermal imaging system costs one-third of the price of competitive systems. The 20-lb, portable unit helps you identify thermal problems in pc boards—the main reason for the premature failure of electronic components.

The thermal imaging system scans a circuit board and produces a full image in approximately 30 sec. The image is displayed on a 5-in. integral monitor using a palette of 16 colors or 16 levels of gray scale. System resolution is 245 × 193 pixels.

The instrument stores one image in memory and lets you use image subtraction to reveal temperature differences between a scanned image and a stored image. Using the software, which comes with the system, you can transmit images via an RS-232C port to an IBM PC or compatible for storage or analysis. Because the unit's infrared detector uses the Peltier effect to cool electronically, there is no need for you to use liquid nitrogen or other inconvenient cooling methods.

The system costs less than competitive systems because it has a slower scan time and because it uses a single oscillating mirror instead of a mulitiple-facet mirror system. Note, however, that the 30-sec scan time is satisfactory for stationary targets such as pc boards.—***Doug Conner***

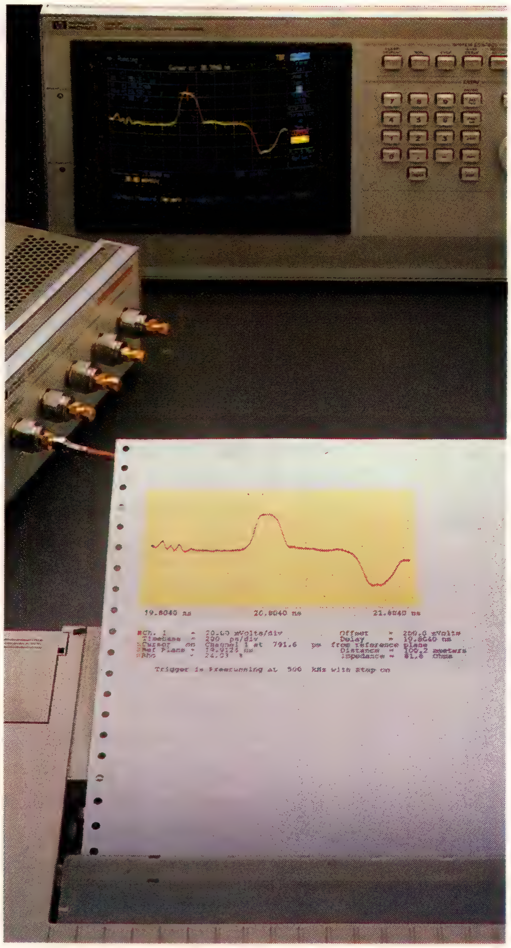
Compix Inc, 7847 SW Mohawk St, Tualatin, OR 97062. Phone (503) 692-6771.

Circle No 727

***This portable thermal imaging system** lets you map pc-board temperatures to identify hot spots that reduce system reliability. You can photograph images with a scope camera or transmit them via an RS-232C port to a computer.*

we never stop asking "What if..."

TDR Yesterday TDR Today



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**Normalization is accomplished using the Stanford Bracewell Transform. The Bracewell Transform is under license from Stanford University.*

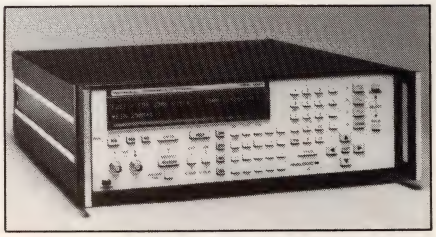
HEWLETT PACKARD

Arbitrary-waveform generators process 800M 8-bit points/sec

Arbitrary-waveform generators, which let *you* define the signals they produce, are based on D/A conversion technology. Some waveform-generation tasks, such as electromagnetic-pulse and radar-return simulation, demand raw speed. When it comes to generating user-definable waveforms at high speed, the 2040 and 2045 excel; they convert data from 8-bit bytes to analog voltages at the rate of 800M points/sec—a value that the vendor claims is the fastest of any arbitrary-waveform generator sold as a standard product. Furthermore, you can obtain an output directly from the signal D/A converters (DACs) and thus take advantage of an amplitude response that is flat within ±2 dB to beyond 200 MHz.

From the front, the new instruments resemble the vendor's Data 2020, an arbitrary-waveform generator that doesn't match the speed of the 2040 and 2045 but which converts with 12-bit precision. Like the 2020, the 2040 and 2045 offer wide latitude in the techniques you can use to describe the waveforms you want the generators to produce. One method is mathematical equation entry. From the units' front panels, you describe the output as an equation, Y = f(t), where f(t) is usually a polynomial expression. In addition, you can download waveforms from a host computer, enter them from sketches you make on a graphics tablet, define them as points or line segments, or recreate waveforms captured by a waveform digitizer or a waveform analyzer, such as the vendor's 6100.

The generators also feature 512k points of memory that you can divide into multiple segments and 78k bytes of battery-backed RAM that



***The front panel of these arbitrary-waveform generators** includes a 2-line alphanumeric display that you use when expressing waveforms as equations.*

stores files containing polynomial waveform descriptions. You can trigger the output waveforms, or you can synchronize or phase lock them to an external source. You can also substitute your own external clock for the ones that are part of the generators.

Both generators provide a pair of analog outputs. The 2040's outputs have an internal impedance of 50Ω to −2V and can supply a 1V p-p signal into a 50Ω load. These two outputs are in phase opposition, and the timing skew between them is ±100 psec. Rise and fall times are less than 500 psec from the 10 to 90% amplitude points. The 2045 takes one of its outputs directly from the main DAC. The other output passes through a programmable 63-dB attenuator; selectable 2- or 20-MHz-cutoff, 3-pole Bessel low-pass filters; and a 275-MHz-bandwidth output amplifier.

The 2040 costs $13,500, and the 2045 costs $14,500. Delivery is less than 90 days ARO.

—Dan Strassberg

Analogic Corp, 8 Centennial Dr, Peabody, MA 01961. Phone (508) 977-3000. FAX 508-531-1266.

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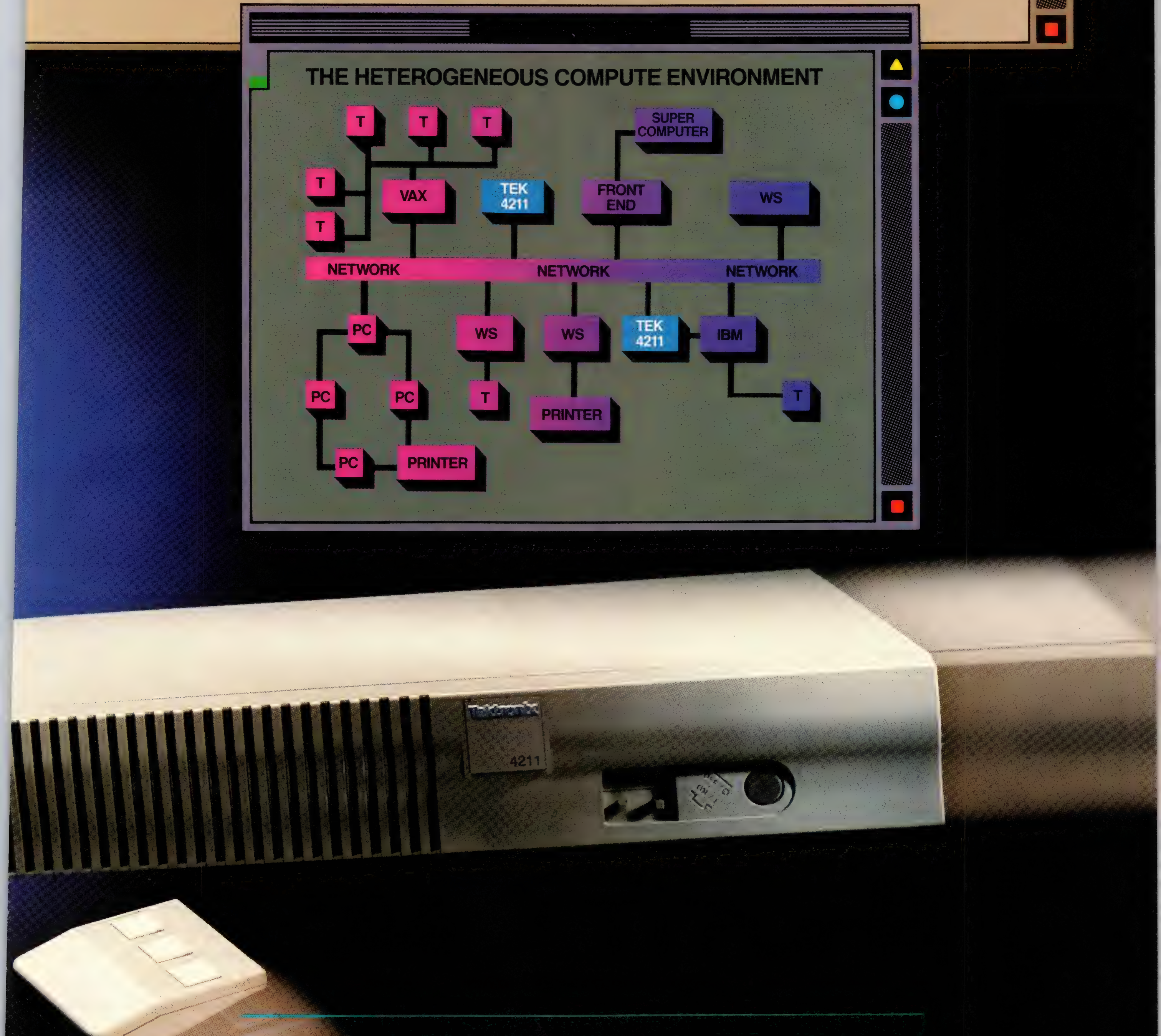

Tektronix

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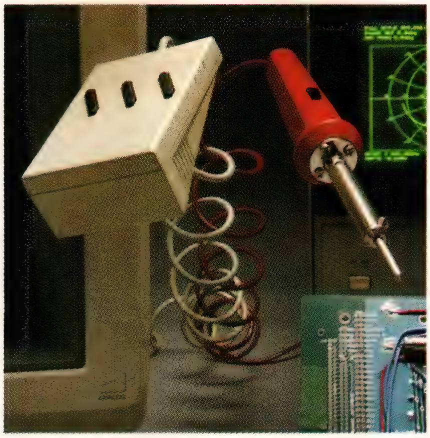


ANALOG simulation

Doug Conner, *Regional Editor*

Analog simulation hasn't yet reached the point where you can use it to design a whole system, but by balancing its use with breadboarding, you can speed up the development process and increase the likelihood of meeting your design specifications on the first try.

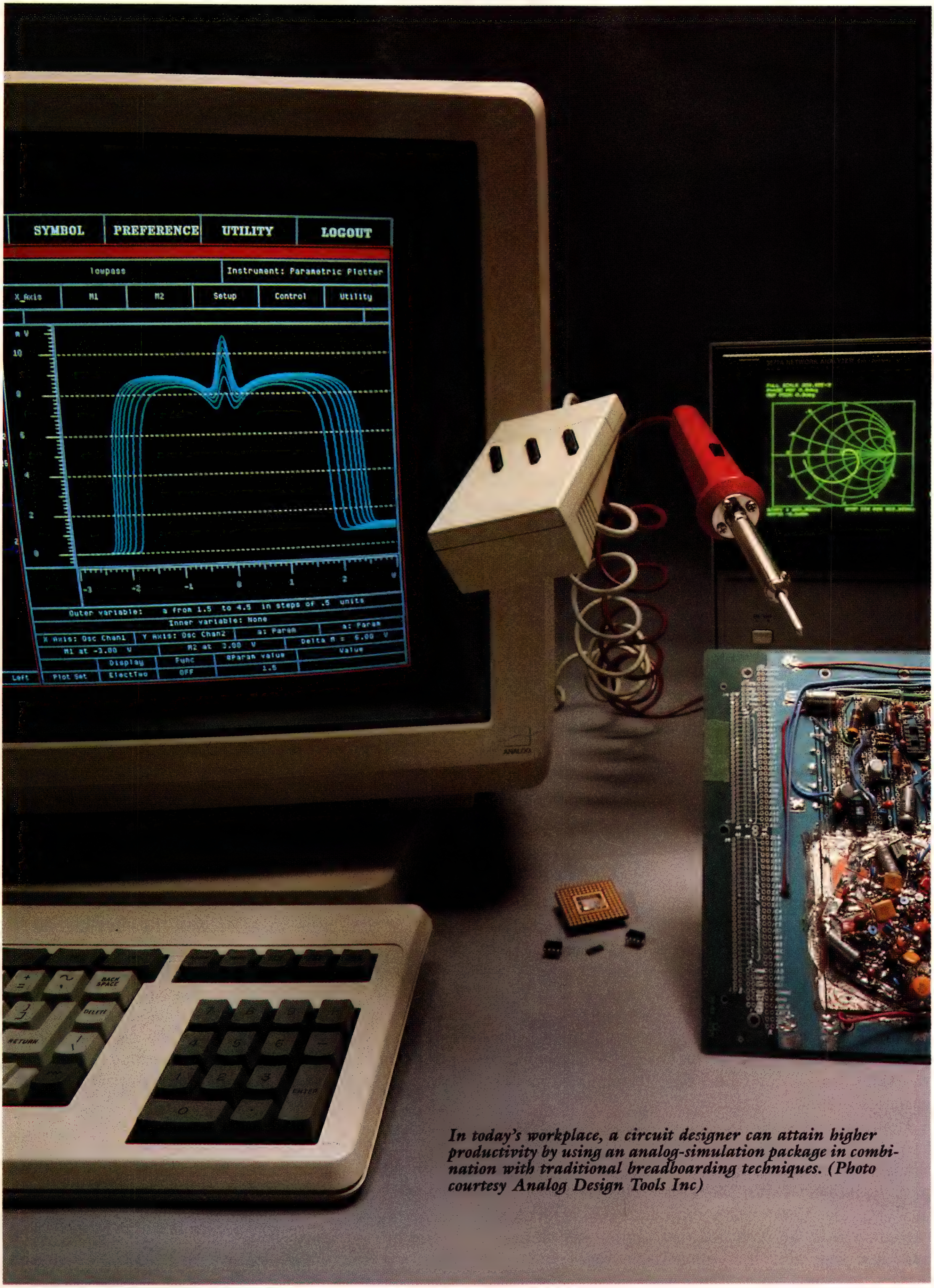
Analog simulation is one of the many tools available to a circuit designer who wants to streamline the design process. Before you can even attempt to use simulation effectively, however, you need to have a realistic perception of what you can expect. Once you decide to try analog simulation, you will be faced with the question of when to simulate during a project, and you'll have to weigh the tradeoffs between breadboarding and simulation. After all, if you simulate a circuit and still perform the same amount of breadboarding, you'll have a hard time convincing your colleagues that you've done anything other than stretch out schedules.

In some cases, you may decide to use simulation for high-level preliminary design work and then switch over to a breadboard. The optimal case is to use simulation at various times throughout the development process, trying for the best match of simulation and breadboarding to edge out the competition by achieving a reliable, producible design that meets your specifications.

You can reduce breadboard iterations

Many designers use some level of circuit simulation in the early design stages because they want to learn more about the circuit before they begin building a breadboard. Simple breadboarding techniques are just not suitable for high-bandwidth components. The introduction of parasitic inductance and capacitance usually requires the construction of production-quality prototypes.

If your design work involves components of this type, simulation may pay off in helping you get the design right the first time. Or, at the very least, it



In today's workplace, a circuit designer can attain higher productivity by using an analog-simulation package in combination with traditional breadboarding techniques. (Photo courtesy Analog Design Tools Inc)

The more you learn at the simulation stage, before you start in with the hardware, the better your chances are that the hardware will work.

***With analog-simulation packages** such as this one from Intergraph, you can look at your simulation results using virtual instruments that simulate the ones you're accustomed to using on your lab bench.*

will reduce the number of expensive and time-consuming prototype iterations required to complete a design. The more knowledge you accrue at the simulation stage before you start in with the hardware—the prototype, finished product, whatever—the better your chances that the hardware will work.

Simulate production variations

Even for those designers who typically develop circuits without using simulation, simulation can help produce designs that are more reliable. Breadboarding does not really address process-variation effects, for instance. An experienced designer will, of course, design a circuit to minimize the effects of process variations. Nonetheless, the ability to simulate such variations can result in a better design evaluation after you think you've done your best to minimize process-variation effects.

Monte Carlo analysis and worst-case analysis are two simulation methods that allow you to look at changes in circuit performance resulting from part-to-part variations within the production tolerances you intend to use. Monte Carlo analysis selects components randomly from an assigned distribution of tolerances and then simulates the circuit using these parts. By making multiple Monte Carlo runs, you can simulate the same distributions that you expect to see during manufacturing. This type of analysis can help if you're designing a board-level product and need to look at the effects of the component variations you can expect from your component vendor's products. Likewise, it's helpful if you're designing ICs and need to look at component variations resulting from your IC fabrication process.

In board-level design, Monte Carlo and worst case analyses have other uses as well. Besides helping to determine if your design will work or how many boards will fail to meet their specifications during a manufacturing run, these types of analyses can show you where you can relax performance specs on an op amp (for example) and still meet your overall performance requirements. Making sure you put premium parts only where you absolutely need them helps keep costs down.

Temperature-stress analysis is a plus

If you're designing circuits for military applications, you will probably have to support your design work with considerable analysis to show that the circuits will work over a wide range of temperatures. The ability to perform temperature-stress analysis with a simulation during the design phase may prevent headaches

The component-modeler capability *of Daisy's Analog Design System lets you modify model parameters and quickly see the effect of those changes. This example shows the effect of changing the output impedance of an amplifier. Modifying models are useful for diagnosing problems.*

later on. Even if you aren't designing for military applications but your circuits need to operate over a wide temperature range, you may very well benefit from temperature-stress analysis.

Analog ASICs and simulation: an ideal fit

If you are an analog-ASIC designer, you are well aware of the prevailing popularity of simulation. Oftentimes, a designer has the option of breadboarding a design using kit parts made with the same process that will eventually produce the ASIC; however, breadboard layout parasitics can totally alter an ASIC design, especially high-bandwidth circuits.

For instance, to take advantage of the high-speed processes available today, such as Tektronix's (Beaverton, OR) Quickchip process (which has 8.5-GHz transistors), you must use simulation. Breadboarding just isn't suitable for developing this type of circuit.

Charles Gopen, VP of marketing at Micro Linear Corp (San Jose, CA), notes that less than 5% of the company's customers breadboard their analog ASIC designs, though they do have access to kit parts if they care to do so. The reason is that few designs can be breadboarded the way they would be integrated on a chip.

An IC designer typically has to design circuits to be insensitive to relatively wide component variations from wafer to wafer. The resistance of metal interconnects on the chip can be significant. The designer can expect the components on each chip to closely match.

Breadboarding dictates a different set of rules. Inductances, which are usually infinitesimal inside an IC (except for bond wires), become a concern. Capacitive coupling can pose problems. Component variation may not be as diverse as it is in ICs, but matching isn't as good either. In short, the differences between designing board-level circuits and designing ICs are significant.

Breadboarding an ASIC is sometimes better

Still, in many cases, breadboarding makes sense. In fact, Raytheon Semiconductor's (Mountain View, CA) RLA linear-array design manual states that breadboarding is absolutely required and Spice computer simulations are optional. Although Raytheon supplies Spice models for those designers who want to perform simulations, the vendor advises that a breadboard will give a closer representation of the eventual circuit (in low-frequency designs). Perhaps equally as important, the designer can use the breadboard within the target system for system-level verification.

Bruce Moore, linear applications engineer at Raytheon and author of the RLA design manual, estimates that about half of Raytheon's customers use Spice simulations as well as breadboarding to develop the RLA arrays. Moore himself uses both Spice simulations and breadboarding.

The manual notes that Spice can be useful in preliminary design, but that it fails to identify latchup modes and often fails to predict local oscillations in emitter followers. Spice also has convergence problems when simulating large circuits. Novice Spice users can further aggravate the problem by making poor assumptions when using Spice and not knowing what problems to look for.

Breadboarding is feasible with Raytheon's linear-array design because the manufacturer provides kit parts of components using the same process as that of the RLA linear array, and critical nodes are confined to these kit parts. In addition, the transistors have a sub-gigahertz bandwidth.

At Harris Semiconductor (Palm Bay, FL), James Spoto, director of semicustom design, says that customers and company engineers alike use simulation for most of their analog-circuit development work, but that they still use breadboarding techniques for very large analog systems and for investigating peculiar problems like breakdown and high-temperature leakage.

Breadboard layout parasitics can totally alter your design, especially in high-band width designs.

Bob Dobkin, VP of engineering at Linear Technology Corp (Milpitas, CA), stresses that it is important to use simulation as a design aid but not to rely too heavily on it: "Simulation is only one of the tools a good engineer uses to determine if a circuit will be manufacturable." Dobkin also agrees that simulation works well in some cases but not in others. For example, simulating a CMOS design provides a good correlation to the hardware, but a bipolar design does not offer such a close match. Dobkin also speaks highly of simulation for high-frequency design: "We couldn't do high-speed designs without it."

Everyone can use sensitivity analysis

Both analog-ASIC and board-level designers sometimes need to tighten up the performance spread of a circuit. They may need to take up slack resulting from part-to-part variations or minimize drift caused by temperature variations. Some simulation packages include a sensitivity-analysis feature that helps you determine which part variations have the most effect on a circuit. Sensitivity analysis lists components starting with those that have the greatest effect on the circuit.

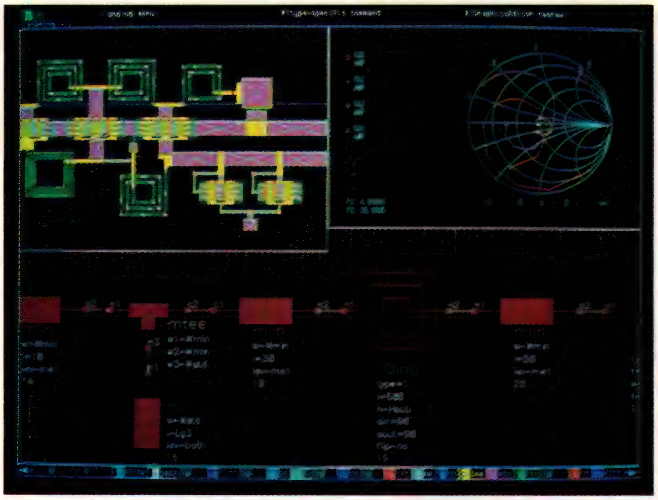
You've got to ask the right questions

What you must remember is that simulation is intended as a design aid and is not meant to do the entire job of designing a circuit for you. In fact, it typically does *only* what you ask. If you're not smart enough to ask the right questions, you may not be aware of lurking problems until after you build your circuit.

Power dissipation is a simple example. If you try to dissipate 2W into an ⅛W resistor, the simulation program probably won't raise a flag, but it will output the value—should you care to ask. A breadboard will show you the error of your ways, no questions asked.

As always, exceptions do exist. Analog Design Tools' simulation package includes a Smoke Alarm feature, for example. The Smoke Alarm indicates when a component has exceeded its ratings. You can also create derated components; the Smoke Alarm goes off when the circuit exceeds that derated value.

In actuality, designing a part into a circuit that could exceed its ratings should be a rare occurrence for an experienced designer. Indeed, a veteran engineer most likely wouldn't be concerned with such simple matters as dissipation. More pressing concerns would include ways of protecting the circuit from destructive short circuits and other extraordinary conditions. One of the benefits of analog simulation is that it can help double-



Optimized for microwave designers, *the MMIC Design Workstation from EEsof comes with the Touchstone simulation package and provides schematic capture, simulation, and layout tools.*

check many simple problems such as these, which a design engineer needs to avoid, and free up time for concentrating on difficult obstacles. Simulators aren't adept at anticipating difficult problems.

You may find it enlightening to think of a simulation package as a tool—just as an oscilloscope is a tool. Both help you find out if a circuit is behaving the way you would like it to. Neither of them helps you fix a problem, but both will show you the effects of your proposed solution.

A simulator and a scope do, of course, have differences. Although an oscilloscope shows how a particular circuit is operating, it may give an inaccurate representation at certain times; scope-probe loading, for example, can alter the function of a circuit. A simulator's portrayal, on the other hand, is limited only by the accuracy of the models that you've used.

Typically, designers that use analog simulation effectively use it as a tool early in the design process and then later on as an aid to help understand what is happening when the simulation and the hardware disagree. In the early stages of design, a simulation package lets you view and analyze a circuit's response as you synthesize the circuit. The simulation provides a method of checking out the circuit to some degree before you actually build a breadboard or before the circuit goes to manufacturing.

When simulation doesn't match hardware

If the prototype circuit works correctly when you build it, you may not have do to any more simulation.

Manufacturers of analog-simulation packages

For more information on analog-simulation packages such as those discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Analog Design Tools
1080 E Arques Ave
Sunnyvale, CA 94086
(408) 737-7300
FAX 408-737-1407
Circle No 625

Analogy Inc
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Beaverton, OR 97075
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FAX 313-663-3640
Circle No 642

Tutsim Products
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Palo Alto, CA 94306
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FAX 415-325-4801
Circle No 643

Venable Industries
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Torrance, CA 90505
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FAX 213-539-4139
Circle No 644

Visionics Corp
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Sunnyvale, CA 94089
(408) 745-1551
FAX 408-734-9012
Circle No 645

Ztec
6745 Lindley Ave
Reseda, CA 91335
(818) 609-8949
Circle No 646

If the simulation and the actual hardware disagree, however, you may very well be perplexed. Assuming that you simulated the circuit correctly (at the very least having modeled first-order effects), several reasons may account for the discrepancy. Second-order effects such as parasitic capacitance or inductance might be the culprit. A model that is incorrect, or one that is correct as far as it goes but oversimplifies the characteristics of a device, may be at fault. Feedthrough or noise coupling that you didn't model in the simulation might be responsible.

Whatever the problem is, you have two choices. You can solve it at the breadboard level—if a breadboard is available—or you can use the simulator to try to find out why the hardware contradicts the simulation.

According to Linear Technology Corp's Bob Dobkin, LTC uses both simulation and breadboarding. When the simulation and the hardware results don't match, the designers use the simulator to determine where the problem lies and they then modify the simulation so that it's correct.

If you're trying to debug an IC, solving your design problem with a simulator might be obligatory. If you have a circuit board, it may be faster to debug the

If you want to take full advantage of the high-performance analog-ASIC processes available today, you'll be forced to use simulation.

problem directly on the prototype board. If you don't go back and make the simulation match the breadboard, however, you won't develop the simulation expertise that'll help you the next time. You'll never sharpen your simulation skills if you resort to breadboarding every time you encounter a problem.

When the breadboard can't survive

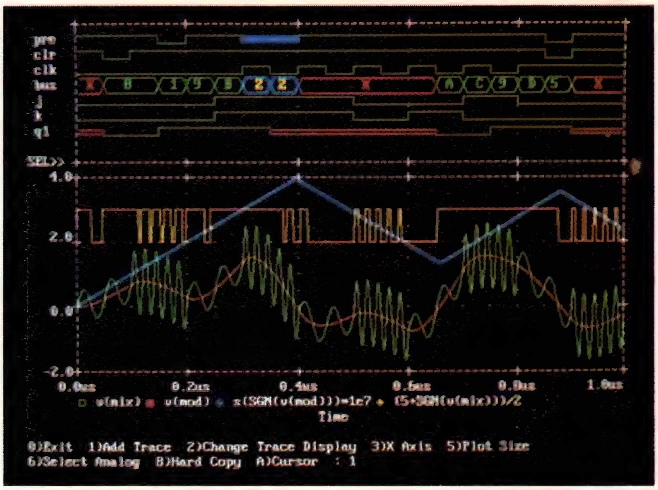
Simulations have distinct advantages over breadboards in solving certain problems. For example, a design flaw in a switching power supply can lead to virtually instantaneous destruction of the circuit when you power up. Experimenting with a handful of power transistors and a storage oscilloscope is not the only way to attack the problem. Performing a simulation with accurate models can permit the circuit to survive the impossible and can bring to light data that explains what is happening in the circuit.

Component models probably present the biggest problem for most users who attempt to get a simulation to match the hardware. Model needs vary greatly from user to user, and no one model of a device can satisfy every application. In board-level design, even if you have a model for the device, it won't necessarily satisfy all your needs because the same device can be modeled at several different levels of complexity. A transistor model may have less than a dozen or as many as several dozen parameters.

If you don't have the necessary model parameters in your library, you'll have to fill them in from data books and parameter analyzers. Many analog-simulation vendors do also sell model libraries. Even if you use one of these model libraries, though, you can still have problems. You need to keep a few things in mind when using model libraries.

When you model a part for a specific application yourself, you can include factors that are important to you in that model. When simulation vendors develop parts libraries, they have to satisfy everyone's needs, which can result in models that are a compromise. A more detailed model than you need will always make the simulation run slower than a simple model. A model that oversimplifies an important effect that you are looking for will cause you even more trouble. In addition, you'll find some variation in the quality of models available, so you need to ascertain the limitations of the model you're using.

You have several means of determining a model's limitations. First, some vendors will describe their models and tell you what has been taken into account



***Mixed-analog/digital simulation** is available on Microsim's latest release of PSpice. Nearly 50 logic primitives accurately represent TTL, CMOS, and ECL families.*

and what has not. Analog Design Tools, for example, publishes data books along with its models that show characteristic device curves; the books detail what effects have been factored in—and the ones that haven't.

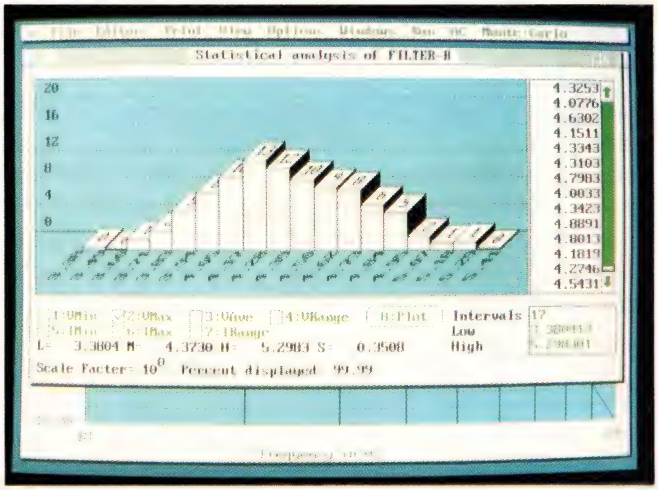
Another good yardstick is to use the model in a simulation of the test circuit shown in the device vendor's data book. Simulating the test circuit allows you to generate your own characteristic curves to see how well the model matches the vendor's data book or to compare your results with those you might have obtained using a parameter analyzer.

You may need to modify a model

If you discover that a model doesn't satisfactorily match the device that you need, you'll have to modify it or make a new one. If you have the source code for the model you are using, you may be able to go in and modify the model to meet your needs. If you don't have the source code, the vendor might provide you with a way to modify the model, but you may not have complete control.

Model modification can also be useful in cases where you want to model a part similar to one for which you already have a model. You may be able to just modify a few parameters and achieve a suitable model.

Sometimes you might just want to try to alter a circuit's performance by experimenting with some model changes. For example, if you think an op amp with a higher slew rate would solve a problem you see in a simulation, you might like to just change that parameter, rerun the simulation, and see if it behaves



Monte Carlo analysis, which is available *on Micro-Cap III from Spectrum Software, lets you look at circuit performance changes resulting from statistical variations in the components.*

the way you expect. Daisy's Analog Design System has a feature called the Component Modeler that lets you make such changes quickly.

Although you have numerous ways of finding a model that's right for your application, device models still present a never-ending problem for board-level-design simulation. As new devices are introduced, simulation users have to go to the trouble of obtaining or developing models of the devices. The only real long-term solution to the problem is to have the device vendors provide models of parts as new parts are introduced.

Precision Monolithics Inc (Santa Clara, CA) has taken the first step in providing Spice models for its new ICs. The availability of simulation models for new parts may become an important issue in the IC community. If you're simulating a design and realize that more than one device is suitable for your application, you'll undoubtedly be swayed to buy from the vendor who provides a simulation model.

When you begin to shop around for an analog-simulation program, be sure to specify the right computer platform for your work. The size of the circuits you need to simulate is probably the primary determining factor in deciding which computer platform is best for you.

Because simulations can take quite a bit of time to run, oftentimes you can't make all the runs that you might like to or that you think is necessary. The best you can do is run the most important cases; considerable engineering judgment is sometimes required to determine just what *is* important.

Using a platform of sufficient speed for your work will enable you to run important cases in a timely manner. Of course, a higher-performance computer costs more and so does the simulator that runs on it. Some vendors offer a designer lots of flexibility by selling different simulator versions that run on machines ranging from IBM PCs all the way up to high-performance workstations and mainframe computers (**Table 1**).

According to Bob Dobkin, Linear Technology Corp runs PSpice on personal computers because the dollars-per-MIPS (multiple instructions per second) figure is better than that achieved with high-priced platforms. Each engineer has his own computer so he has better control of the schedule; there is no mainframe to bog down because of multiple users. Management gave the LTC engineers a choice—to buy expensive workstations and put several engineers on each, or give each engineer a personal computer—and the preference for the latter was overwhelming.

Because LTC is an IC manufacturer, it develops its own models for devices used in the manufacturing process; the company has no need for a simulation vendor that supplies a large device model library; it creates its own.

Val Garuts, chief engineer at Tektronix's Electronics System Laboratory (Beaverton, OR), uses Intusoft's Spice program and runs it on a PC. Garuts designs ICs for a fabrication process having 16-GHz transistors. Breadboarding is useless for the circuits he designs. Typical circuit sizes are on the order of tens of transistors; the maximum limit is about 100. Garuts estimates that simulations typically take about a minute on his 386-based system, and he finds this speed adequate. Although he has access to high-performance computers, his design work generally doesn't require them.

If you need to simulate large designs, for either an IC or a board-level design, you'll need the processing power of a workstation or possibly a mainframe, and even on these, large simulations may run slowly.

Integrated packages may be your choice

If your department or company has already acquired a substantial number of workstations, you'll probably want to run your simulations on those. Ideally you want your analog-simulation package to mesh seamlessly with your other electronic design automation (EDA) software. **Table 2** lists some of the simulation software available from EDA vendors.

Using a simulation package supplied by a broad-line

A model that oversimplifies an important effect that you are looking for will cause you a great deal of trouble.

EDA vendor can sometimes provide a cleaner flow from schematic capture to simulation to board layout. Tight coupling between the schematic-entry software and the simulator makes circuit entry and modification painless. You should note that three of **Table 1**'s simulation vendors are also broad-line EDA vendors: Daisy, Intergraph, and Mentor Graphics.

As you evaluate analog-simulation programs further, you'll find other considerations that are also important. Most analog CAE programs use Spice or a Spice derivative. Many of the derivatives modify Spice's model equations to improve Spice's shortcomings in converging on a solution.

Modeling a device in a Spice simulation requires both model equations and model parameters. Model equations describe device types and technologies. For example, a simulator would have different model equations for silicon bipolar junction transistors and FETs. These model equations are part of the simulation software and the user typically cannot modify them. Model

TABLE 1—REPRESENTATIVE ANALOG-SIMULATION PACKAGES

VENDOR	PRODUCT	PRICE	COMPUTER PLATFORM	SIMULATOR	BEHAVIORAL MODELING	MODEL GENERATION SOFTWARE	TEMPERATURE-STRESS ANALYSIS
ANALOG DESIGN TOOLS	ANALOG WORKBENCH	$15,000 TO $60,000	A, H, I, S	ENHANCED SPICE	✓		✓
ANALOGY	SABER	$15,000 TO $60,000	A, D, S, ALLIANT	SABER	✓	✓	✓
BV ENGINEERING	ACNAP	$125	I, M	PROPRIETARY	✓	✓	
COMPACT SOFTWARE	MICROWAVE HARMONICA	$17,500 TO $25,000	A, D, H, I, S, MANY MAINFRAME COMPUTERS	PROPRIETARY		✓	✓
DAISY	ANALOG DESIGN SYSTEM	$29,000 TO $57,000	D, S, DAISY LOGICIAN	ENHANCED SPICE		✓	
EESOF	TOUCHSTONE	$9900 TO $14,000	A, D, H, I, S	PROPRIETARY		✓	
ELECTRICAL ENGINEERING SOFTWARE	PRECISE	$9500 TO $54,000	A, D, I, S	ENHANCED SPICE	✓	✓	✓
IMAGINE THAT	EXTEND	$495	M	PROPRIETARY	✓	✓	
INTERGRAPH	CSPICE	$10,000	INTERPRO WORKSTATIONS	ENHANCED SPICE	✓	✓	✓
INTUSOFT	IS SPICE/386	$386	I (386 BASED)	ENHANCED SPICE			
JENSEN TRANSFORMERS	COMTRAN	$2850	H, I (WITH HP BASIC CARD)	PROPRIETARY	✓	✓	
MENTOR GRAPHICS	MSPICE	$9900	IDEA STATION	ENHANCED SPICE		✓	✓
META-SOFTWARE	HSPICE	$8000 TO $90,000	A, D, H, S, MANY MAINFRAME COMPUTERS	ENHANCED SPICE		✓	
MICROSIM	PSPICE 4.0	$950 TO $11,900	D, I, S, M	ENHANCED SPICE	✓	✓	✓
RLM	NETOPT	$2000 TO $4000	D, I	PROPRIETARY			
SOFCAD	LINCAD	$159	I, M	PROPRIETARY	✓		
SPECTRUM	MICRO-CAD III	$950 TO $11,900	I	PROPRIETARY		✓	✓
TATUM LABS	ECA-2	$675 TO $3000	A, I, M	PROPRIETARY	✓		✓
TUTSIM	FANSIM	$395	I	PROPRIETARY	✓		
VENABLE INDUSTRIES	MODEL 220	$15,000 TO $22,000	I	PROPRIETARY		✓	
VISIONICS	ANALOG SIMULATOR	$495	I	PROPRIETARY			
ZTEK	ZSPICE	$300	I	SPICE			

NOTES: A = APOLLO D = DEC VAX H = HP I = IBM PC/XT, PC/AT M = APPLE MACINTOSH S = SUN

parameters model specific device types within a technology; the user can alter these. It is the model equations that vendors often modify to improve Spice convergence.

Although many vendors of Spice-related simulators claim to have improved convergence compared with standard Berkeley Spice versions, most users maintain that problems remain. Knowing how to conquer convergence problems is still what differentiates the novice Spice user from the experienced one.

MONTE CARLO/ WORST-CASE ANALYSIS	MIXED-ANALOG/ DIGITAL SIMULATION	COMMENTS
✓		LARGE LIBRARY, NONLINEAR MAGNETICS, SCHEMATIC ENTRY
✓	✓	
✓		
✓		RF AND MICROWAVE DESIGN, LINEAR AND NONLINEAR SIMULATION, OPTIMIZATION CAPABILITY
✓		DATA SHEET MODELER, MAGNETIC CORE LIBRARY, LIMITED MIXED-SIGNAL CAPABILITY
✓		RF AND MICROWAVE DESIGN
✓	✓	
	✓	FLEXIBLE BLOCK-DIAGRAM SIMULATOR FOR PRELIMINARY DESIGN
✓		LARGE MODEL LIBRARIES AVAILABLE
✓		RUNS IN PROTECTED MODE, USES EXTENDED MEMORY
✓		LINEAR-ANALYSIS PROGRAM, OPTIMIZATION CAPABILITY
✓		
✓		OPTIMIZATION CAPABILITY
✓	✓	
✓		LINEAR NETWORK DESIGN, OPTIMIZATION CAPABILITY
✓		LINEAR ANALYSIS
✓		LIMITED MIXED-SIGNAL CAPABILITY
✓		
		FFT FREQUENCY ANALYSIS AND SIMULATION
		INTEGRATED SIMULATION AND MEASUREMENT FOR SERVO AND POWER-SUPPLY DESIGN

Mentor Graphics is attempting to overcome the problems of convergence by using more model equations and will offer a major modification to Spice early next year. The company also plans to build up a high-quality component library by using component testing and parameter extraction. The initial release will include an 1800-component library, and the company will issue quarterly releases thereafter.

You should also be aware of the availability of analog-simulation packages that are dedicated to specific design specialties. EEsof and Compact Software, for example, are two analog-simulation vendors that have developed tools dedicated to RF and microwave design.

Analogy's Saber is a simulation package that allows you to perform system-level simulations. Saber is more than just an analog-circuit simulator, however. You can use both standard electronic-device models and standard mathematical equations to define elements (electronic, mechanical, and chemical) of a complete system.

Mixed-mode simulation is on the rise

Following the system-level-simulation concept, in May Analogy and HHB (Mahwah, NJ) announced a system-level mixed-analog/digital simulation program. The package combines Analogy's Saber with HHB's Cadat. The mixed-mode simulation capability is especially important for circuit designs that have feedback paths linking analog and digital circuits.

You'll also be able to get system-level and mixed-mode simulation capability with Microsim's PSpice version 4.0, which is scheduled for release this month. Version 4.0 includes a behavioral-modeling capability that allows you to describe functions either with equations or look-up tables. The Digital Simulator Extension (DSE), an event-driven, 28-state logic simulator, provides the mixed-mode simulation capability.

Linear analysis is fast

You'll also find linear-analysis programs available. Linear-analysis programs run fast and give good results, provided that you can live with the restrictions of linear analysis. Comtran, a linear-analysis program from Jensen Transformers, has some useful features. John Youngquist, president of Insight Instruments (Fort Erie, Ontario, Canada), uses Comtran simulations in conjunction with actual hardware from other parts of a system to develop circuits. Youngquist uses a digital scope to digitize a circuit waveform and sends

The only real solution to the model problem is to have the device vendors provide models of parts as they introduce them.

TABLE 2—THIRD-PARTY SIMULATORS USED BY EDA VENDORS

VENDOR	SIMULATOR
CADENCE (SAN JOSE, CA)	HSPICE, SPICE
CADNETIX (BOULDER, CO)	SABER
CASE TECHNOLOGY (MOUNTAIN VIEW, CA)	HSPICE, PSPICE
COMPUTERVISION (BEDFORD, MA)	ANALOG WORKBENCH, SABER
HEWLETT-PACKARD (PALO ALTO, CA)	ANALOG WORKBENCH
ORCAD (HILLSBORO, OR)	PSPICE
PCAD (SAN JOSE, CA)	PSPICE
RACAL-REDAC (WESTFORD, MA)	SABER
VALID LOGIC SYSTEMS (SAN JOSE, CA)	PRECISE
VIEWLOGIC (MARLBORO, MA)	HSPICE, PRECISE, PSPICE, SABER, SPICE

the waveform over an IEEE-488 link to the computer he uses for simulation. By passing the digitized waveform through a Comtran filter simulation, he can view the filtered waveform on the computer or perform further spectral analysis. Using this method, a designer can examine how a filter performs with real data before he begins to build it.

What will the future hold?

When high-level managers look at the improvements in productivity that have resulted from digital simulation, especially in IC design, they often think that stepping up the use of analog simulation is the way to arrive at corresponding dramatic improvements in analog-design productivity. This attitude often glosses over the complex differences between digital and analog design.

Looking at just two aspects of analog simulation will illustrate these differences. Two primary concerns in many analog-design situations are noise coupling and parasitic RLC, both of which are related to the physical layout of a board. Noise problems don't exist in digital design as long as the noise is below threshold (unless you are concerned with the picosecond differences that noise causes in transition times). Similarly, a digital designer can usually ignore layout-related parasitic RLC, provided that it is kept within reasonable bounds. Usually a digital designer following good design practices need not worry about noise and parasitic RLC.

In contrast, the analog designer—whether an IC or a board-level designer—will always see the effects of noise and parasitic RLC degrading the performance of a circuit. It is not sufficient for the analog designer to use good design practices; high-performance circuits require careful attention. At present, analog simulation does not handle either noise coupling or parasitic RLC very well. Both problems require expertise on the part of the engineer. You can enter the parasitic RLC values as part of the circuit description, but no simulator exists that will automatically feed these layout-induced RLC values back into the simulation.

Learning to use any new tool requires you to take time out to learn how to use it. This holds true whether the tool is simple to use, such as a digital storage oscilloscope, or whether it is something complex like an analog-simulator program. If you've been procrastinating about using analog simulation in your design work, you should weigh the pros and cons carefully, and think about the future. If you see analog ASICs in your future, you'll find it even more important to learn how to use analog simulation effectively—before the stakes become even higher. EDN

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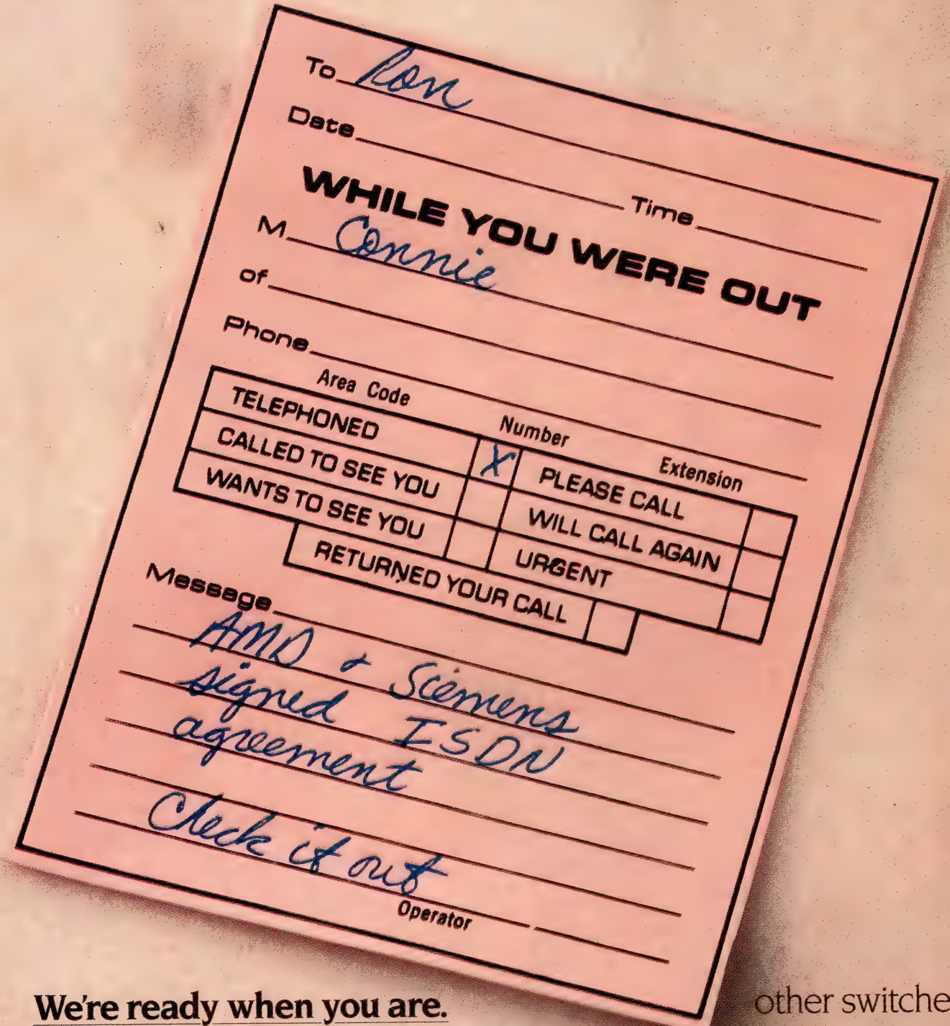

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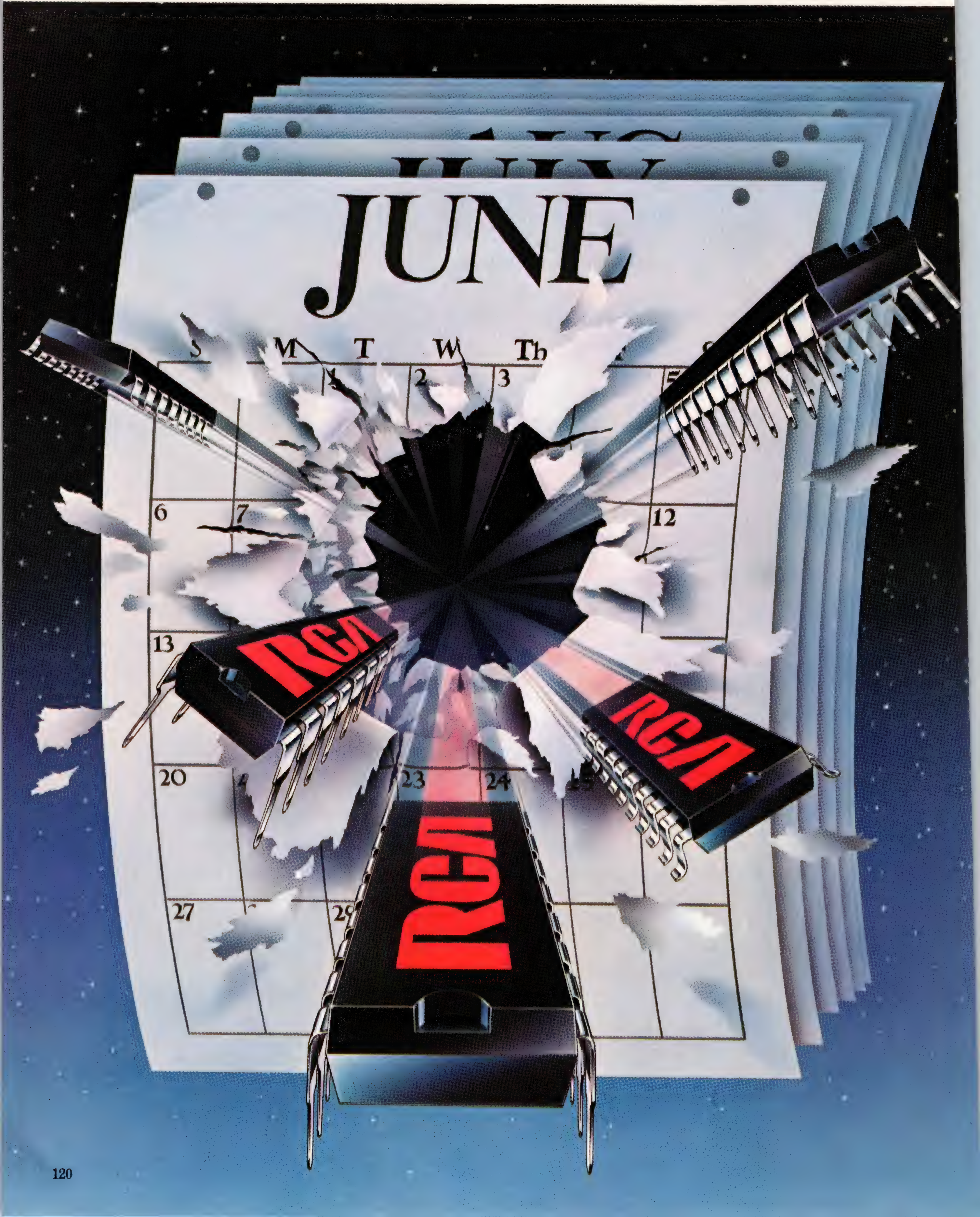

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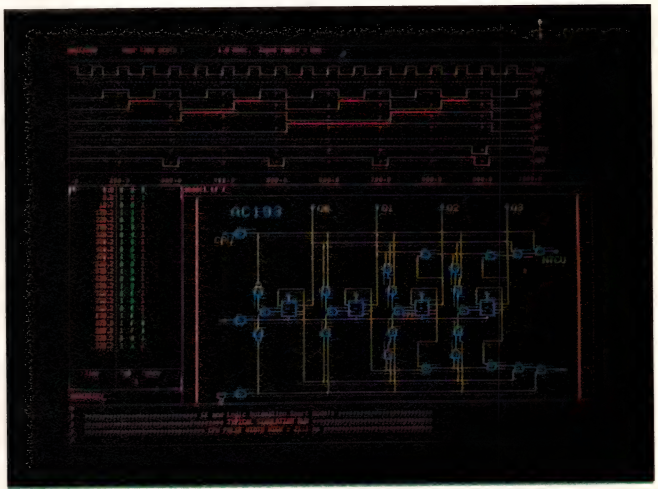

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RISC design woos 32-bit-μP architects

RISC is not a fad or an obscure religion, but a technology that follows the prime tenets of the computer industry; future 32-bit μPs will incorporate at least a few RISC concepts.

Steven H Leibson,
Regional Editor

Although reduced-instruction-set computer (RISC) design is often perceived as unconventional, in fact it adheres strictly to the first commandment of the computer industry: Thou shalt go faster. It's true that many people promote RISC architectural design with religious fervor, but RISC ideas are definitely not faddish. RISC's originators derived some of the fundamental concepts of the design philosophy by carefully analyzing millions of lines of existing computer code. The analysis indicated that most of the software in use at the time (the late 1970s) did not make optimal use of the CISC (complex-instruction-set computer) processor hardware. Although the problem still exists for CISC processors, the RISC concepts developed from that research caused a major course correction that will influence all computer architectures and systems for years to come.

RISC design traces its roots to the first electronic computers. These early computers were direct-execution machines that had simple, easy-to-decode instruction words. Consider the IBM 360 computer family, which the company introduced in 1964. Every member of this family executed the same instruction set, but the lower-cost machines didn't contain sufficient processor hardware to directly execute every instruction in parallel fashion.

A ghost in the machine

Instead, these smaller machines reused hardware resources over several clock cycles to execute complex instructions incrementally. A small "machine within the machine" supervised this piecemeal instruction execution. Because instruction execution required several clock cycles or states, each of these small states was dubbed a microstate, and the control program that supervised the incremental instruction execution became known as microcode.

Microcode caught on like wildfire, because microcoded machines require less processor hardware and reduce main-memory bandwidth re-

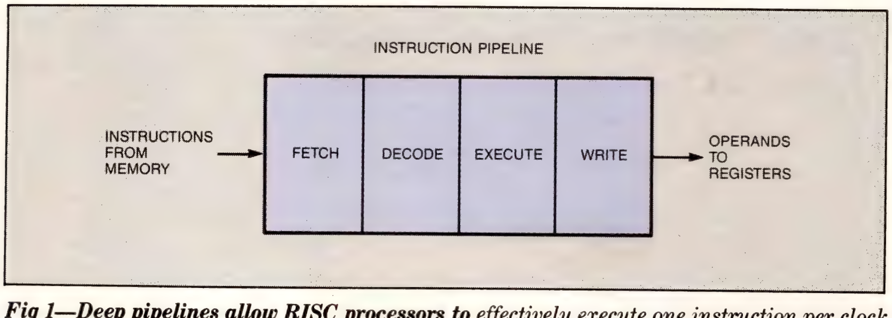
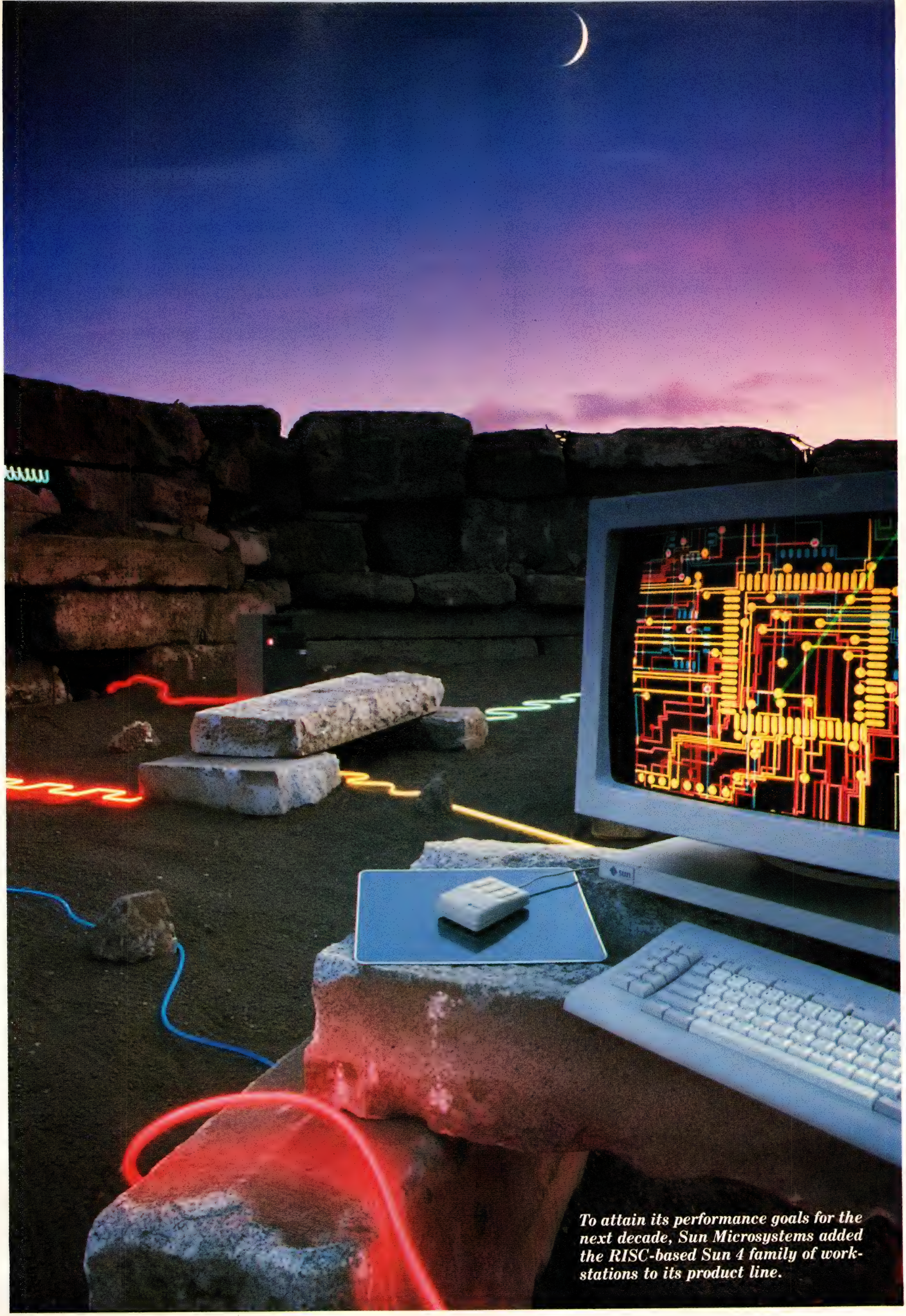


Fig 1—Deep pipelines allow RISC processors to *effectively execute one instruction per clock cycle. This pipeline from the Sun Microsystems SPARC processor has four stages: The fetch stage acquires an instruction from memory; the decode stage decodes the instruction, fetches the appropriate operands from the register file, and generates the next instruction address for the fetch stage; the execute stage performs arithmetic and logical operations; and the write stage places the results of the computations back in the register file.*



To attain its performance goals for the next decade, Sun Microsystems added the RISC-based Sun 4 family of workstations to its product line.

quirements. At a time when you could buy four gates in an IC and main computer memories were being built from relatively slow magnetic cores, both of these benefits were very important to computer designers.

Minicomputer designers warmly embraced microcode as a way to build cost-effective machines. They especially needed to reduce hardware costs and boost performance. In the technology of the day, small microcode stores built from ROM and microstate machines were definitely a way to achieve those goals. In fact, microcode design became a high art in the hands of the minicomputer designers. Fixed, ROM-based microcode stores gave way to RAM-based, writable control stores, which made the task of removing microcode bugs easier and allowed an elite cadre of minicomputer application programmers to optimize a computer's instruction set for each program.

Microcode suited early μPs

Microcode also filled the bill for early μP designs. The first μPs had 4- and 8-bit data paths that forced designers to use multiple word instructions. These processors required microcoded state machines to accommodate an instruction's multiple words. The continued success of microcode design made the technique a permanent entry in the processor architect's lexicon.

When μP data paths grew to 16 bits, processor designers built upon the foundations of the first μPs, using larger microcode ROMs and more elaborate microstate machines. The increasing power of these microcode machines allowed processor architects to create increasingly elaborate instruction sets with a large number of addressing modes.

At the same time that the 16-bit μPs started to appear, software managers started turning to compilers as a means of alleviating the growing software crunch. Although hardware was becoming easier to design, thanks to rapid improvements in semiconductor technology, the associated software projects failed to meet deadlines as program size swelled. Engineers became more ambitious—they wanted to solve tougher problems with microprocessors that required ever larger, more complex programs. During the 16-bit-μP wars of the late 1970s, all the μP vendors claimed that their products' elaborate instruction sets were ideal for compiled code, but their assertions turned out to be untrue.

Matching compilers to processors

In 1975, a group of researchers led by George Radin at IBM's Thomas J Watson Research Center started work on a computer based on concepts developed by John Cocke, who advocated compilers that used simple instructions. The researchers looked at many millions of lines of compiled code and made a surprising discovery. Although elaborate instructions are helpful to human assembly-language programmers, compilers largely ignore them. Compiler writers simply didn't take advantage of the enhanced CISC instruction sets, because the complex CISC instructions often did not perform a task precisely as needed. Rather than using a complex instruction and cleaning up undesired side effects with additional code, compiler writ-

Capable of accommodating four RISC processors, *the DN10000 Personal Supercomputer from Apollo Computer employs a 64-bit instruction word that's split into 32-bit integer and floating-point segments.*

ers usually elected to use the simpler instructions that produced no side effects and were easier to control.

The IBM researchers determined that most of the code produced by compilers consisted primarily of load, store, branch, add, and compare instructions, and that these simple instructions had direct microcode equivalents. Further, the researchers observed that many of the more complex minicomputer instructions they examined did not require much extra hardware to execute the complex instructions, they just added microcode to the microcode ROM. The investigators concluded that you really don't need a microcode store and a state-machine controller in your processor if you construct a computer that executes one instruction per clock cycle; the processor instructions replace the microcode. These findings guided the creation of IBM's experimental 801 computer, which the company completed in 1979. The IBM 801 is generally recognized as the first RISC machine.

By the beginning of the 1980s, rumors of the 801 project spread even without formal disclosure by IBM. In 1980, David A Patterson of the University of California at Berkeley started work on "RISC I," a VLSI implementation of a RISC processor. He subsequently built an improved version, RISC II. John Hennessy, at the Computer Systems Laboratory at Stanford University, started the design of the MIPS (microprocessor without interlocked pipe stages) μP in 1981. Both projects produced working μPs, but Patterson's "RISC" name stuck and became the generic name for the design philosophy.

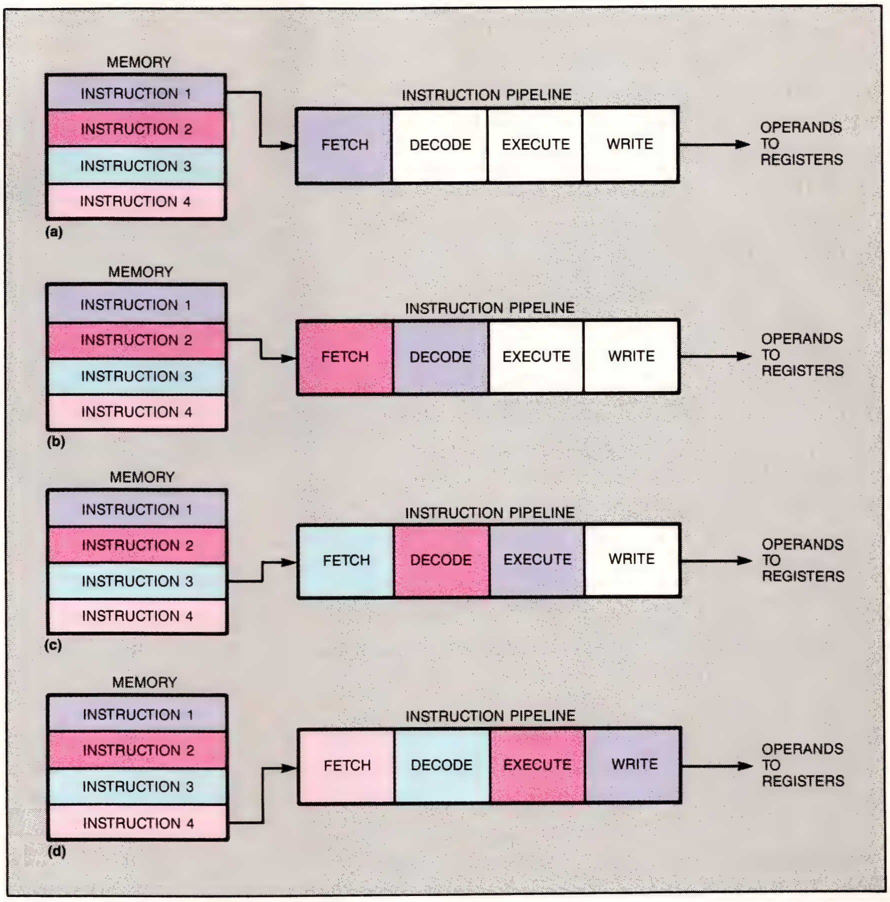


*Fig 2—**The SPARC pipeline holds as many as four instructions** in various stages of execution. After an instruction is fetched **(a)**, it passes through the subsequent decode **(b)**, execute **(c)**, and write **(d)** stages at the rate of one stage per clock cycle. If the processor can keep each stage filled, the average instruction time (AIT) will be one clock cycle.*

RISC is a misnomer

Unfortunately, though, the term "reduced-instruction-set computer" is somewhat misleading. The goal of RISC-based design definitely is not to reduce the number of executable instructions. Rather, the main objective of RISC design is to create a high-speed computer by making the compiler and processor a matched set. The RISC processor should be simple, with a minimum number of logic stages, so that it will run as fast as any given semiconductor process technology allows. In addition, the processor should have a variety of instructions to support the needs of the compiler, but no more instructions than the compiler requires. Additional instructions require extra transistors and gates, which are simply excess baggage.

If you view the RISC design philosophy as a cult (some do), you'll note that the religion has several sects and many boisterous prophets. Most of them agree on a few things, however. For example, most RISC proponents state that a RISC processor should have at least several of the following characteristics:

- Single-cycle instruction execution
- Fixed-length instructions
- Load/store architecture
- Large register sets
- Delayed branches
- Support for high-level languages.

Pure RISC processors have no microcode: The machine's instructions become the microcode. Because there is no microcode or microstate machine, the average instruction time (AIT) for a RISC processor should be one instruction per clock cycle; however, no real μPs yet attain that goal. Deep pipelining **(Fig 1)** allows a RISC processor to execute an average of one instruction per clock cycle, even though each instruction actually consumes many clock cycles **(Fig 2)**.

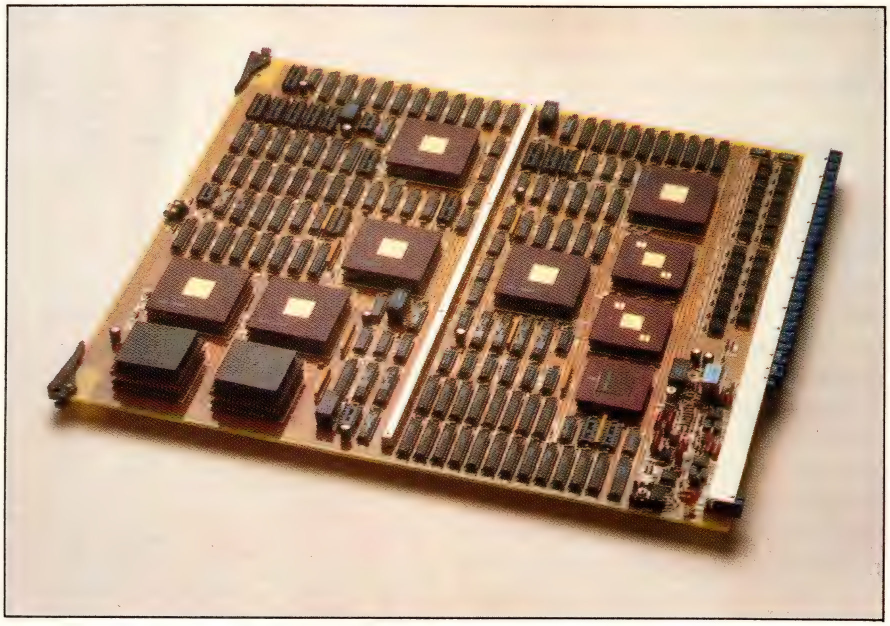
Achieving an AIT of one instruction per clock is the key to RISC performance. Flip-flops built with a particular semiconductor technology support a certain maximum clock rate. A 1-instruction/clock processor extracts every iota of performance from any particular IC process. In contrast, CISC processors that require several cycles to execute an instruction dilute the maximum clock rate of a fabrication technology. Thus, say RISC proponents, a RISC processor can always run faster than any CISC processor built with the same semiconductor process.

A RISC processor has no microcode to interpret instructions; it must directly decode every instruction in one clock cycle. A fixed-length instruction simplifies this task. In addition, RISC processors need fixed-length instructions to minimize the pipeline complexity.

In a pure RISC implementation, only the load and store instructions move data between the processor and memory. This approach reduces the number of addressing modes to one or two, further simplifying processor design and maintaining the processor's ability to execute an average of one instruction/cycle.

A large register set reduces a program's need to store operands in external RAM. Because access to external memory is generally slower than access to processor registers, a large register set allows a program to keep operands readily available; it also reduces memory-bandwidth requirements.

RISC processors have large pipelines to satisfy the computer's voracious appetite for instructions and to break up the instruction-decoding and -execution stages. Thus, the processor fetches instructions several cycles before actually executing them. In a conventional pipelined processor, a branch or jump to another area in a program invalidates the remaining instructions in the pipeline and forces the pipeline controller to flush the pipe. Fetching instructions that are subsequently flushed from the pipeline before they can be executed wastes as much as 20% of the computer's memory bandwidth.



Together, the integer and the floating-point unit *on the Apollo DN10000 RISC processor board can execute as many as three instructions simultaneously.*

To counteract this effect, a RISC processor delays the execution of a branch for several cycles after decoding the branch instruction. This delay allows the execution stage to supply the pipeline controller with the proper address for the instruction following the branch. The problem with this approach is that the pipeline controller must put something into the pipeline immediately following the branch instruction to keep the pipeline busy until the proper instruction can be fetched. Optimizing compilers tailored to RISC machines generally attempt to move calculations that would logically occur before a branch to a position following the branch instruction. A delayed-branch architecture always executes the instructions that immediately follow the branch, so it will produce identical results whether the processor executes the calculations before or after executing the branch instruction.

RISC processors are nightmares to program in assembly language. The deep pipelines, simple instructions, and delayed branches can tax even the best assembly-language programmer. Because the RISC instructions are the machine's microcode, you often need many more RISC instructions than CISC instructions to perform a given task. The simple RISC instructions make the compiler's job easy, however, because the choice of instructions is limited. Thus, RISC-processor designers select instruction sets to favor compilers over human assembly-language programmers.

RISC μPs emerge from the lab

IBM's 801 never became a commercial product. The RISC and MIPS university projects, however, ignited a RISC revolution. Sun Microsystems Inc based its SPARC architecture and Sun 4 family of workstations on Patterson's RISC work; Patterson acted as a consultant on the project. Hennessy helped found MIPS Computer Systems to commercialize the MIPS architecture.

Semiconductor vendors have since introduced a wave of RISC, "near-RISC," and "RISC-like" μPs. In fact, the term "RISC" has become the industry's latest buzz

word for processors with widely varying architectures, so you may see the label "RISC" on many products that only partially conform to the RISC philosophy.

The principles underlying the RISC design philosophy have profoundly influenced computer-system design. RISC's biggest effect is a leap in memory-bandwith requirements. Because a RISC processor executes approximately one instruction per clock cycle, it needs a new instruction from memory at almost every clock cycle. Standard memory subsystems based on today's dynamic-RAM (DRAM) technology simply can't achieve this performance level for the fast processors that today's semiconductor technology makes possible.

Instead, high-performance RISC systems almost universally use cache memory to provide a buffer between the voracious appetite of the RISC processor and the somewhat more sedate abilities of a dynamic-RAM-based memory subsystem. Computer-system designs based on the latest, high-speed versions of CISC μPs such as the 68020 and 80386 μPs are also starting to use cache memory, so the advent of RISC designs merely accelerated an existing trend (**Ref 1**).

RISC μPs from AMD, Intergraph APD, and Motorola incorporate separate 32-bit data paths for instructions and operands (a Harvard architectural configuration) to relieve this memory-bandwidth bottleneck. The dual data buses not only relieve the bandwidth problems, but also allow you to integrate two separate caches in a system design. Often, the instruction and operand buses merge on the opposite side of the cache memories, so that one bulk-memory subsystem can supply the needs of both data streams (**Fig 3**).

The processors in Apollo Computer's DN10000 Personal Supercomputer employ just such a dual-cache approach. On the basis of empirical trials, engineers at Apollo elected to build operand and instruction caches of different sizes. Each DN10000 processor incorporates a 64k-byte data cache and a 128k-byte instruction cache. The DN10000's caches are asymmetrical, because Apollo's engineers found that, in general, a computer's processor performs more instruction fetches than data transfers.

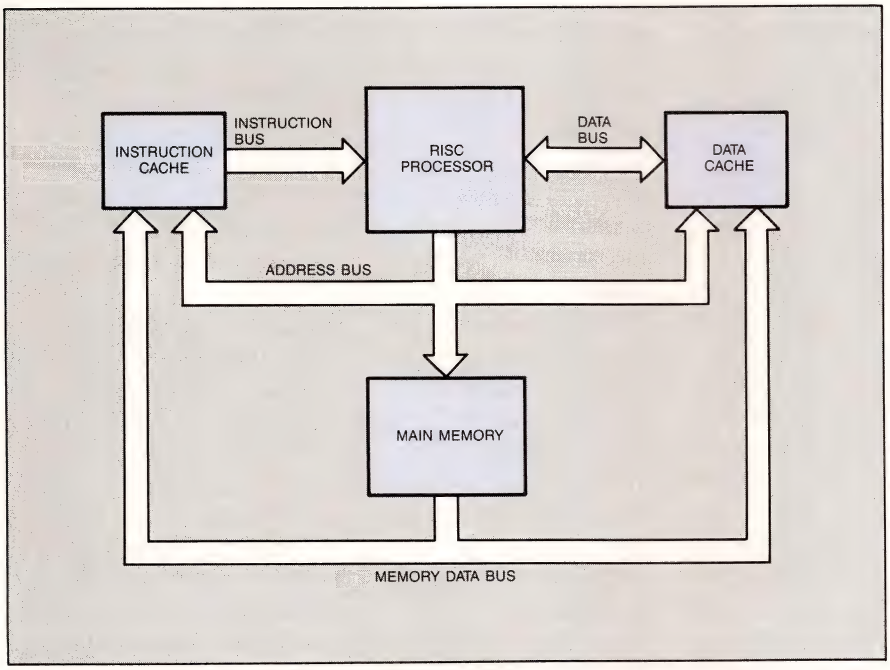


***Fig 3—Because RISC processors have high memory-bandwidth requirements,** many RISC-based systems employ separate data and instruction buses (a Harvard architecture) to improve the total bandwidth into the processor. Dual buses also allow you to incorporate dual cache memories in your design.*

AMD also attacked the memory-bandwidth problem in a manner that lets you make a tradeoff: You can build a system that doesn't have cache memory, but has better performance than a conventional DRAM-based design might ordinarily supply. The AMD 29000 can fetch instructions in variable-length bursts by sending out one address and then reading subsequent data and instruction words without using the address bus. Thus, you can use a little extra circuitry to efficiently couple this μP to page-mode, static-column-access-mode, or video DRAMs, and use these devices' burst-access modes to produce a much lower average memory-access time.

Note that this burst-access feature does not preclude the use of cache memory for designs that require greater performance. Systems that require maximum performance can employ static RAM as bulk memory, but you would generally reserve that approach for cost-insensitive applications. For large memory subsystems, cache-assisted DRAM designs perform almost as well as memory subsystems built entirely from static RAM, but they cost much less per byte.

Cache-memory size becomes even more of an issue for RISC-based systems, because RISC compilers generally create larger programs than CISC compilers do. Estimates of the code inflation caused by the simplicity of RISC instruction sets range widely, from 40% growth to expansion by a factor of 3. Remember that a RISC instruction set is, in effect, the RISC processor's microcode, so many operations that are integral to CISC instructions (operations such as automatic incrementing, for example) must be explicity performed by additional RISC instructions.

Generally, this code expansion

does not detract from the RISC processor's execution speed. However, floating-point computations are one exception to that rule. Processor designs that adhere closely to strict RISC philosophies do not perform floating-point calculations quickly, and commercial RISC μPs either employ floating-point coprocessors or boost performance by putting floating-point units on the same chip with the integer unit. To be fair, many CISC μPs don't perform floating-point calculations all that well, either. In fact, many RISC designs use the same Weitek or Texas Instruments floating-point coprocessors that CISC-based systems often use.

Although the underlying concept of a RISC design is processor sim-

Lies, damn lies, and benchmarks

"There are three types of lies:" wrote British prime minister Benjamin Disraeli, "lies, damn lies, and statistics." Benchmark programs, which generate computer-performance statistics, have accumulated an air of significance as absolute indicators of CISC and RISC computer speed. We try to ease our selection among several alternative computer architectures by running benchmark programs on specific implementations of candidate architectures and comparing the results. We hope that by reducing the choices to a few simple numbers, we can make the best decision with minimal pain.

Unfortunately, decisions based on standardized benchmarks are built on quicksand, but that fact hasn't stopped computer vendors from crowing about the latest favorable benchmark results, often without bothering to explain the methods or the programs used to obtain those results.

For example, the simplest and most frequently cited performance numbers associated with RISC machines are the millions of instructions per second (MIPS or native MIPS) that the processor can execute. You can easily obtain this theoretical value by multiplying a processor's average instruction time (AIT) by its clock rate (assuming that the processor operates in a zero-wait-state environment). Computer-science experts discourage the use of the MIPS yardstick, because the number gives you no clue as to the real amount of work a system performs. The AIT is an average based on some imaginary combination of instructions for a "typical" application. In addition, most RISC designs employ hierarchical memory comprising cache and bulk storage, so they don't run at zero wait states all the time.

By definition, the average RISC instruction does less work than an average CISC instruction, so a MIPS rating gives you only partial information. The MIPS spec is analogous to engine RPM in a car: The tachometer tells you how fast the engine is running, but without knowing the transmission setting, you can't determine how fast the car is going.

In an attempt to compensate for the varying work capacities of RISC and CISC instruction sets, some well-meaning souls (who shall remain nameless) introduced the concept of the IQF (instruction quality factor), which rates an instruction set's work capacity in relation to the instruction set of the Digital Equipment Corp (Concord, MA) VAX 11/780 minicomputer. The team arbitrarily gave the VAX's instruction set an IQF of 1. Supposedly, you can multiply a processor's MIPS rating by its IQF to arrive at an absolute measure of processor speed; however, no standard for deriving IQFs exists.

Many vendors, therefore, have switched to another contrived performance metric called VAX MIPS. When Digital Equipment Corp introduced its VAX 11/780 minicomputer, the company claimed the computer executed 1 MIPS. Purveyors of the latest wave of 32-bit RISC and CISC μPs, workstations, and computers often cite VAX MIPS ratings to indicate how fast their products perform tasks. These vendors often provide two numbers—one for integer performance and one for floating-point performance.

If you use VAX MIPS ratings to compare competing products, you'll want to unearth the methodology that was used to generate the results, because there is no standard suite of programs for determining VAX MIPS. You should also understand that the VAX 11/780 doesn't actually execute 1 MIPS. Its performance was clocked at 0.47 MIPS in 1984 **(Ref 1)**. Still, you can use VAX MIPS as a relative measure of performance, as long as you understand and agree with the methodology used to obtain the ratings.

You can also choose to employ benchmark programs that have become the de facto standards frequently used to measure computational performance. Among these, the Dhrystone, the Whetstone, and the Linpack seem to be the most common. These three programs are written in various high-level languages (HLLs), so you must understand that each result derived from these benchmarks indicates the combined performance of a specific hardware system implementation and a particular version of a compiler. This situation should cause you to cast a jaundiced eye on published benchmark results for any particular μP, because the system implementation and the compiler also affect the outcome.

plicity, prices for RISC-based systems start to climb when you tack on such items as fast memory, one or two cache memories, and a floating-point coprocessor. RISC-based computers and workstations occupy the high ends of product lines from vendors that offer both RISC- and CISC-based designs (Apollo Computer, Hewlett-Packard, and Sun Microsystems, for example). Thus, you won't soon see RISC design invading the low-end and cost-sensitive applications currently dominated by 8- and 16-bit μPs.

Another reason that RISC processors aren't descending into the 8- and 16-bit realm is the smaller word width. Generally, 8- and 16-bit data paths are not wide enough to accommodate a fully decoded RISC

According to Paul Bemis, a senior product manager at Apollo Computer, the Dhrystone, Whetstone, and Linpack benchmarks form a performance triathlon for high-performance computer systems. He asserts that you can't tell how a computer will perform from the results of any one of the three programs, but that the system that delivers the best balance of performance results for all three benchmarks will provide the best overall throughput.

The Dhrystone benchmark program tests a computer system's integer performance. It was originally created by Reinhold P Weiker at Siemens AG (Erlangen, West Germany). He wrote versions of the Dhrystone program in Ada, Pascal, and C. Rick Richardson of PC Research Inc (Tinton Falls, NJ) later translated the original Ada version into another C-language version. Thus, there are several iterations of the Dhrystone program running about.

Early versions of the Dhrystone program performed computations and never used the results of those calculations. Some compiler optimizers recognized this situation and didn't bother to generate code for calculations that produced "useless" data. Superior compiler technology, therefore, resulted in very fast program execution times and worthless Dhrystone results. To obtain reasonable benchmark numbers on these early Dhrystone programs, you turned off the optimizer. That step further clouded the comparison between RISC and CISC machines, because RISC processors rely heavily on program optimization for significant performance improvements. The latest Dhrystone programs, version 2.0 and higher, use the results of all the calculations to rectify this problem. If you give any credence to Dhrystone ratings, you should ask what program version was used to obtain the results.

The Whetstone benchmark tests floating-point performance. Apollo's Bemis claims that the Whetstone provides a measure of scalar floating-point performance. However, Sun Microsystems asserts that the Whetstone benchmark program actually contains a mixture of floating-point and integer arithmetic, array indexing, function calls, conditional jumps, and transcendental functions, so it doesn't deliver a good indication of scalar floating-point performance. MIPS Computer Systems concurs, stating that the Whetstone benchmark has been carefully arranged to defeat vectorizing and many compiler optimizations. The company also notes that several versions of the Whetstone program appear to be in use, causing people to report different results for the same machine.

Jack J Dongarra at the Argonne National Laboratory (Argonne, IL) developed and maintains the Linpack benchmark program. The program, written in Fortran, measures the time required for a computer to solve a 100×100 matrix of linear equations. The Linpack benchmark measures program-execution times for both single- and double-precision computations and reports performance in millions of floating-point operations per second (M flops).

In an attempt to unify the jumbled status of benchmarks by acting as a central repository, The National Institute of Standards and Technology (NIST, formerly the National Bureau of Standards) in Gaithersburg, MD, maintains a collection of benchmark programs for testing computers. You can obtain these benchmarks over Arpanet (**Ref 2**).

In the final analysis, standardized benchmarks can't tell you how well a computer system or processor architecture will perform for your particular application. Only your application program will tell. For future projects, therefore, consider writing your software in a transportable high-level language (HLL) as a first step. You can then use that program to help you select the most appropriate hardware for the job. RISC processors are especially suited to this approach, because they're designed to take maximum advantage of HLLs.

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2. Wakid, Shukri, "NBS response," *Computer*, September 1988, pg 69.

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instruction in one transfer, and multiple-word instructions are anathema to the RISC philosophy. The Harris RTX-2000 μP is an exception, because it employs a stack-based architecture instead of the more conventional, register-based RISC approach.

The RTX-2000's stack architecture allows the μP's instructions to use implied operand addresses. Most 32-bit RISC instruction sets incorporate fields for three operands that explicitly address two source registers and one destination register. Each of these explicit references requires a certain number of bits in the instruction word. Some instruction sets use as many as eight bits per register address (consuming 24 bits of the 32-bit instruction) just to specify the operand sources and destination.

The RTX-2000 uses no bits to specify operand addresses, because its stack architecture makes addresses implicit. A 16-bit instruction word suffices, therefore. The unusual architecture of the RTX-2000 arises from the high-level language the Harris designers selected. The RTX-2000 directly executes Forth, a stack-based programming language; the μP's architecture reflects this choice.

Some companies claim that the RISC design approach makes no more sense for 32-bit machines than it does for 8- and 16-bit ones: They cite well-publicized benchmarks that show equal or superior performance by CISC designs (see **box,** "Lies, damn lies, and benchmarks"). However, the topic of computer benchmarks is a minefield; you should be careful not to rely on canned benchmarks too heavily. Unless you know exactly what abilities a benchmark emphasizes, the results can easily mislead you.

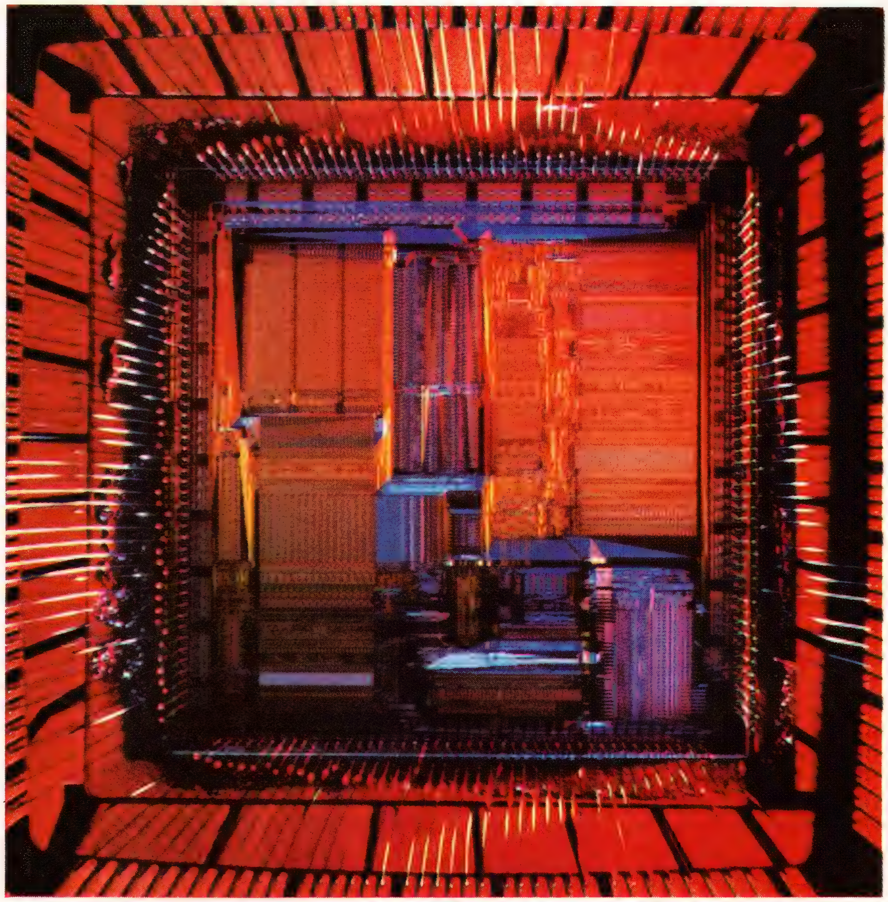
Benchmarks may prove nothing

For example, according to Wayne Rosing, vice president of advanced development at Sun Microsystems, two often-cited benchmarks indicating that the 68020-based Sun 3 performs as well or better than the SPARC-based Sun 4 actually measure the rotational velocities of the systems' hard disks and the systems' VME Bus transfer rate, respectively. Clearly, it would be foolish to use that sort of data in choosing between CISC and RISC. Rosing cites the Sun 4's performance on a "real" program: the Verilog ASIC simulator from Gateway Design Automation Corp (Lowell, MA). One particular Verilog simulation, which runs in 8 to 9 hours on a Sun 3 workstation, runs 2.51 times faster on the Sun 4.

In addition, several μP vendors caution you not to confuse any processor's architecture (whether RISC or CISC) with a particular system implementation of that architecture. Many factors beyond processor architecture—including clock rate, cache size, main-memory size and bandwidth, and I/O-bus bandwidth—influence overall system performance.

Compilers control performance

One factor that plays a major role in determining RISC-based system performance is not hardware at all—it's the compiler. This situation isn't specific to RISC processors; it applies to CISC processors, too. Assuming that the hardware remains constant, you can observe performance differences of as much as 30% or more simply by changing from one vendor's compiler to another's or from one language to another. RISC-based-computer and -workstation vendors such as Apollo, Hewlett-Packard, and MIPS developed their RISC processors and compilers simultaneously to opti-



Comprising 160,000 transistors, *the Motorola MC88100 RISC μP incorporates integer and floating-point execution units and features separate instruction and data buses to overcome memory-bandwidth limitations.*

mize the match between the processor architecture and the compiler.

These companies categorically assert that you achieve maximum performance from a RISC architecture by closely tying the hardware design to the development of an optimizing compiler. This opinion echoes the findings of the early RISC researchers, who discovered that CISC compilers, developed long after the introduction of the associated processor, didn't use many of the μP's instructions. The tenets of RISC philosophy bar the inclusion of instructions that the compiler won't exercise. The circuitry required to decode and execute these superfluous instructions represents a waste of silicon that might be better allocated for speed-enhancing features such as floating-point units or bigger on-chip cache memories.

Assembly language bites the dust

Note that this philosophy, for better or worse, consigns assembly-language programming to the great technological dustbin. Because of this disregard for assembly-language programming and a closely related indifference to existing assembly-language software, RISC dissenters do exist, but they argue more with the relatively inconsequential aspects of pure RISC theory than they do with RISC's goals. Greater processing speed is still the primary objective, and everyone agrees that executing one or more instructions per clock cycle is a good idea.

Edge Computer (Scottsdale, AZ), one of RISC's dissenters, has almost achieved one instruction per clock cycle by using the instruction set of Motorola's 68000 μP family instead of a "reduced" one. The company makes computers based on a board set that emulates the instructions of the Motorola 68000, 68010, and 68020 μP. Edge used several RISC design techniques such as pipelining, a 5-bus Harvard

RISC μPs herald 32-bit alternate sourcing

Beyond its architectural benefits, RISC technology has finally ushered in the era of multiple sources for 32-bit μPs. All the old-line μP vendors have kept their respective 32-bit CISC architectures proprietary and have remained the sole sources for these parts. Two RISC architectures, however, the Sun Microsystems SPARC and the MIPS Computer Systems MIPS, were developed by companies that focused on building systems rather than chips. These companies actively sought multiple sources for their RISC μPs. As a result, you can buy chips based on these two architectures from several companies.

Integrated Device Technology Inc (IDT) offers the R2000 and R3000 μP chip sets, which are based on the MIPS architecture. The firm has a 10-year agreement with MIPS Computer Systems to develop enhanced versions. LSI Logic Corp also offers the R2000 and R3000 chip sets as standard products. In addition, LSI Logic offers the MIPS CPU core as a megacell in its ASIC library. Performance Semiconductor Corp also offers the MIPS chip sets. ICs from all three vendors are mutually pin compatible.

Like MIPS Computer Systems, Sun Microsystems has taken measures to ensure the availability of its SPARC architecture. The company's philosophy in licensing SPARC, however, is to encourage licensees to produce a range of products that offer various price/performance levels. Sun doesn't require the licensees to produce pin-compatible parts. Five semiconductor vendors, including Bipolar Integrated Technology, Cypress Semiconductor, Fujitsu Microelectronics, LSI Logic, and Texas Instruments, either offer or plan to offer various SPARC devices. Bipolar Integrated Technology, which obtained a SPARC license in 1987, is developing parts based on its ECL manufacturing process.

Fujitsu supplied Sun with SPARC ICs for its Sun 4 workstations and became the first semiconductor vendor to market SPARC parts. Fujitsu built the first integer unit (IU), called the S-16 (denoting 16.7-MHz operation), by using 1.5-μm gate-array technology. The company has since introduced a faster part, the 25-MHz S-25, which is based on a 1.2-μm fabrication process. For floating-point calculations, Fujitsu's integer units couple to Weitek's WTL1164 floating-point multiplier and WTL1165 floating-point ALU.

The 179-pin S-25 does not plug into existing S-16 sockets; however, LSI Logic has announced plans to offer a SPARC μP that's pin compatible with Fujitsu's S-25. LSI Logic will also offer a SPARC processor that is pin compatible with the 33-MHz CY7C601 SPARC IU offered by Cypress. Texas Instruments plans to offer a SPARC IU that plugs into CY7C601 sockets as part of a 5-year alternate-sourcing agreement with Cypress. In return, Cypress receives the right to make and market a version of TI's 74ACT8847 floating-point unit (FPU), which augments the integer capabilities of the CY7C601.

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architecture, and cache memories to boost the performance of Motorola's μP architecture. Edge simply ignored the RISC goals of fixed-length instructions and a load/store architecture, because these features didn't allow the company to maintain compatibility with the 68000. As a result, Edge's original Model 1000 CPU achieves an AIT of 1.6, and the second-generation Model 2000 CPU has an AIT rating of 1.4.

Like Edge Computer, semiconductor vendors marketing CISC μPs are not oblivious to the benefits offered by the RISC design philosophy. The truth is, every 32-bit microprocessor introduced from now on will most likely exhibit RISC features as well as architectural enhancements such as multiple on-chip execution units. An Intel spokesman, discussing the design of the company's recently introduced 80960, put it this way: "We adopted the RISC philosophy without converting to the religion."

RISC design influences CISC μPs

Indeed, the Intel 80960 is a good example of a 32-bit μP that was introduced after RISC ideas became widely published. The processor has a load/store architecture, 3-operand instructions, a 512-byte instruction cache, and a large register set. However, the 80960 also incorporates microcode. The microcode not only interprets complex 80960 instructions, it allows the processor to execute a power-on self-test without fetching instructions from memory, something microcodeless RISC μPs can't do.

Intel's 80960 architecture also contains multiple execution units. The announced parts have one integer and one floating-point execution unit, but the company plans to extend the architecture by adding additional execution units to future 80960 family members. Many RISC vendors predict that processor ar-

Manufacturers of RISC μPs and workstations

For more information on RISC μPs and workstations, circle the appropriate numbers on the Information Retrieval Service card, contact the following manufacturers directly, or use EDN's Express Request Service.

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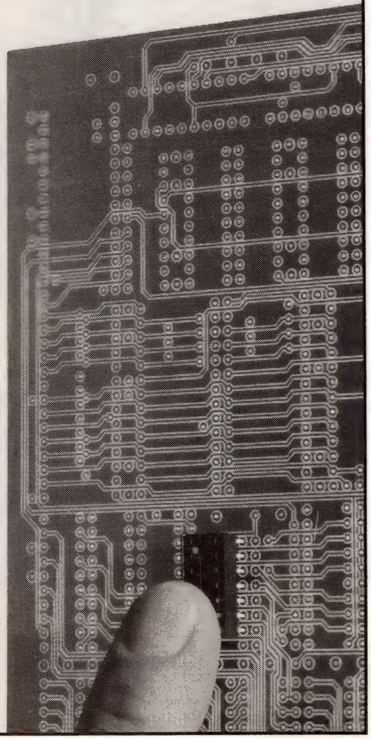

chitects will soon widely use multiple-execution units, operating simultaneously on one chip, to drive a processor's AIT below 1. Motorola often points out this same possibility when discussing the architecture of its 88000 RISC μP.

Whether you join the RISC faithful or not, the RISC design philosophy shows no signs of diminishing in popularity. For 32-bit μPs and compiler-based programming environments, RISC processors deliver added speed. Further, as several companies have already discovered and proved, RISC design techniques can provide many performance benefits without discarding the benefits of CISC design for those who "adopt the philosophy without converting to the religion." EDN

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3. Gimac, Charles E, and Veljko M Milutinović, "A Survey of RISC Processors and Computers of the Mid 1980s," *Computer*, September 1987, pg 59.
4. Lilja, David J, "Reducing the Branch Penalty in Pipelined Processors," *Computer*, July 1988, pg 47.
5. Wharton, John H, "Architecture vs Implementation in RISC Wars," *Microprocessor Report*, August 1988, pg 14.

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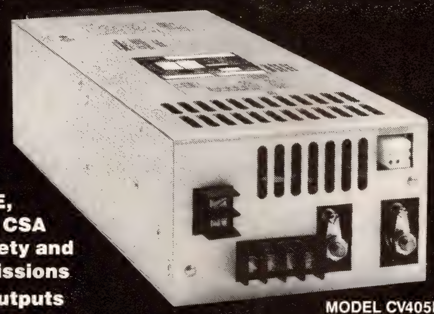
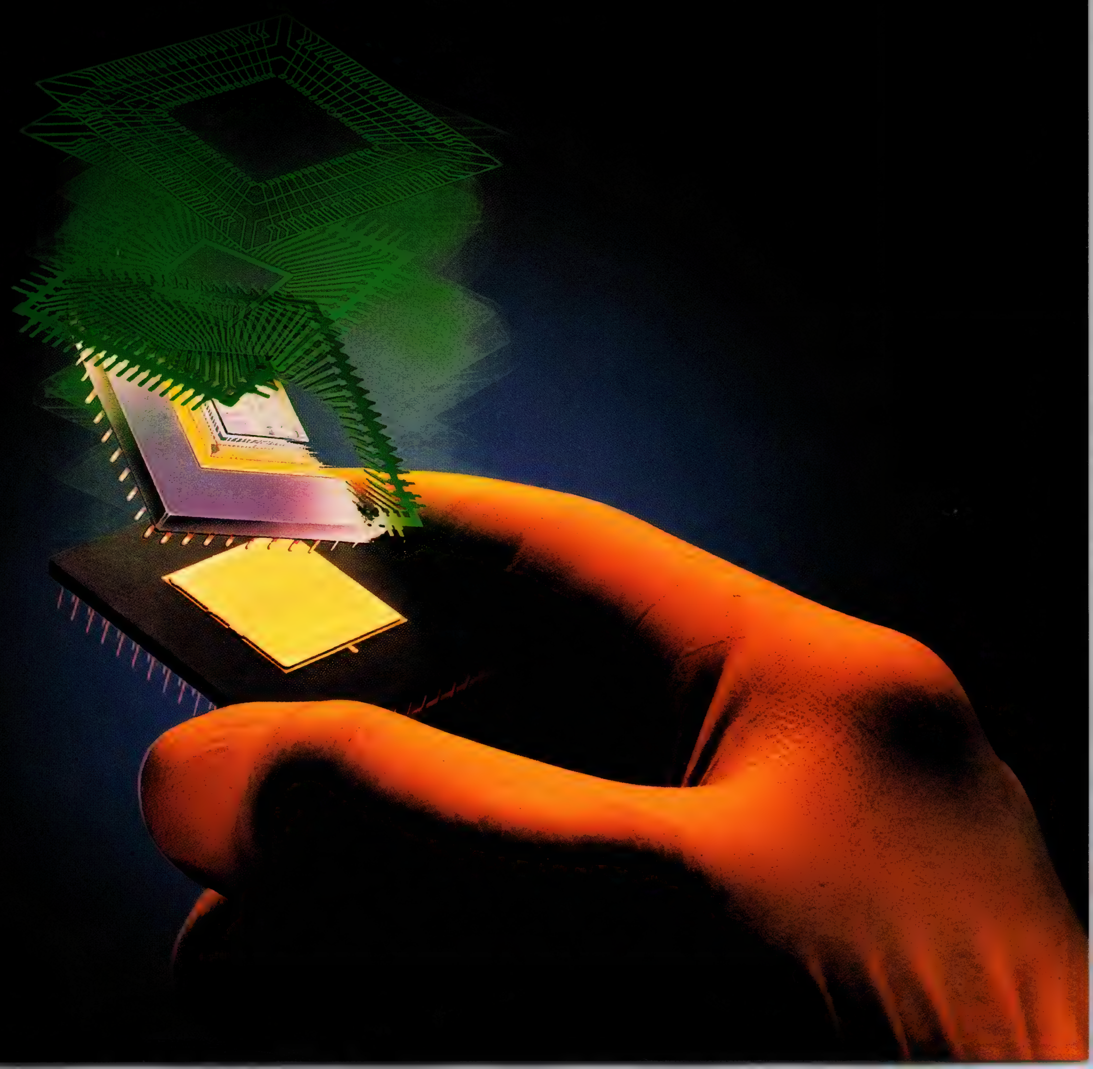


TEXAS INSTRUMENTS REPORTS ON GRAPHICS

IN THE ERA OF MegaChip TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

Why do industry leaders graphics processors from

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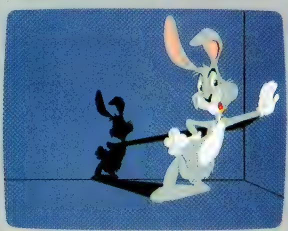

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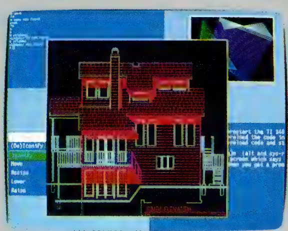

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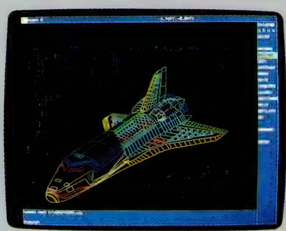


Matrox

National Design, Inc.

NEC Home Electronics

pick industry-leading Texas Instruments?

Stretching across the bottom of these pages is but a fraction of the hundreds of systems based on TI's industry-standard TMS340 graphics family. At the left is a Sun-3 utilizing TI's leadership '74ACT8800 building-block processor family. Which only goes to prove designers choose TI graphics products for everything from workstations to PCs, from laser printers to arcade games.

They get design options that allow them to differentiate their products and to better tailor price and performance to their markets.

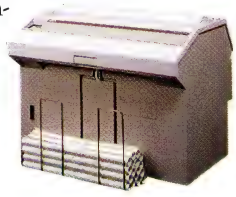
They also move to market faster with less risk. TI graphics products are proven, available, fully supported—the standard by which others are measured.

Let a few of the designers tell you about their choices:

"The TMS34010 was the only graphics processor that could meet the performance requirements of our laser plotter controller."

—*Al Sabel, Advanced Products Manager, Xerox Corporation*

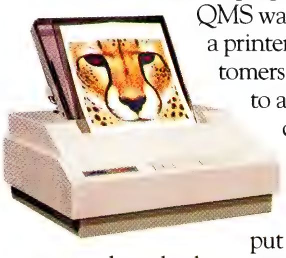
The Xerox 8836 had to produce D- and E-sized drawings with a resolution of 400 dots per inch at a constant speed of one inch per second. The 34010 delivered: Six million instructions per second with a "draw" rate of up to 50 million pixels per second.



"The programmability and architecture of the TMS34010 provide the performance and flexibility we need for color- and graphics-intensive printer products."

—*Dr. Donald Parker, Exec. V.P. Products & Technology, QMS, Inc.*

Because the 34010 is programmable, QMS was able to build a printer that their customers could program to accept scanned color input and to provide high-speed color output as well as hard copy with multiple printer support.



"TI's ACT8800 technology allows our TAAC-1 application accelerator to significantly boost the computing power of a Sun workstation for imaging and graphics applications."

—*Nick England, Director Application Accelerator Group, Sun Microsystems, Graphics Products Division*

"The 8800's power lets us combine the functionality of an image processor, an interactive graphics device, and an array processor in a single product and still offer user programmability."

There's more in store from the ACT8800 family. The recently disclosed 8847 floating-point processor combines two 64-bit functions on a single chip: A floating-point multiplier and a floating-point arithmetic logic unit. Its number-crunching capability: 33 MFLOPS.

"In designing graphics systems, you can't forget about tomorrow. And TI hasn't."

—*Carl Calabria, Director of Engineering, Truevision® Inc.*

"The 34010 enables our True Vista® video graphics boards to bring workstation performance to IBM® compatibles and Mac IIs. It is the only graphics chip that will allow us to migrate our applications software to even higher-performance second-generation TMS340-based systems." *See road map on next page.*

The TMS340 second-generation processor is three to 20 times faster than the 34010. It is user configurable, software and plug-in compatible.

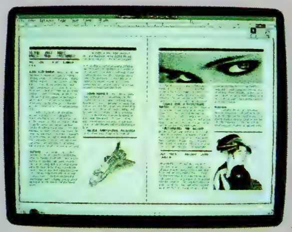
Two other products designed in parallel with the new TMS340 processor are the One-Megabit Video RAM and the industry-first floating-point graphics processor, with on-board, high-level graphics instructions.

The One-Megabit VRAM enhances the performance of the 34010. And when used in tandem with the second-generation processor, performance is improved up to 50 times over other processor/VRAM combinations.

The floating-point graphics processor executes up to 40 MFLOPS and interfaces directly with the address and data buses of the second-generation TMS340, allowing it to perform computation-intensive functions more than 10 times faster than current PCs.

For details on TI's software and third-party support, turn the page.

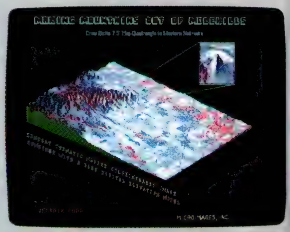
RasterOps



Renaissance GRX

Truevision

Vermont Microsystems



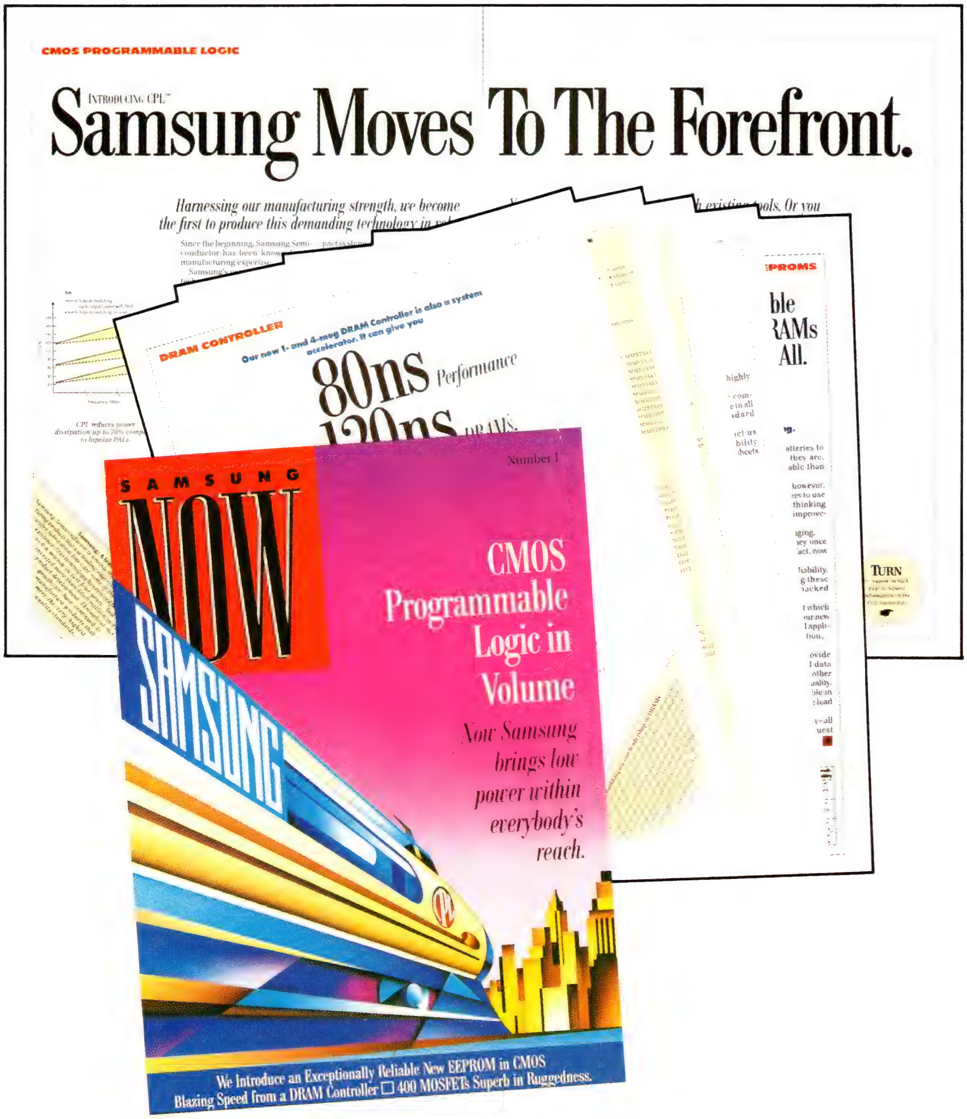
Vectrix

PRESENTING THE WINNING ADVERTISEMENTS

From EDN Magazine Edition's August 4, 1988 Issue

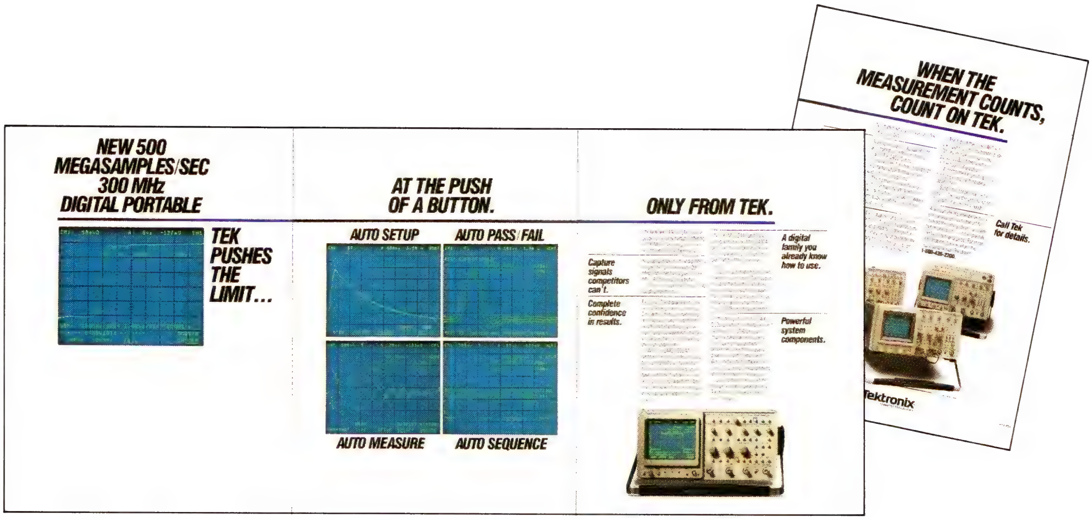
Here are the winning advertisements from EDN Magazine Edition's August 4, 1988 Reader Vote Contest. Our readers analyzed and evaluated the advertisements in the issue to select the ones they judged to be the most informative, helpful and attractive. Congratulations to the advertisers and agencies who combined well-written copy and superior design to create these winning advertisements. A special thank you to the readers who took the time to participate. Here then are the outstanding performers

FIRST



- **COMPANY: Samsung Semiconductor**
- **AGENCY: Neil Ransick Marketing Services**
- *"Colorful, informative and demands attention."*
  Manufacturing Engineering Manager, Digital Equipment Corporation
- *"Extremely good graphics and text. Good product data."*
  Development Engineer, A T & T Bell Laboratories
- *"Just perfect: Impressive, informative. Interesting close."*
  Designer, P.A.Toma

FIRST RUNNER-UP



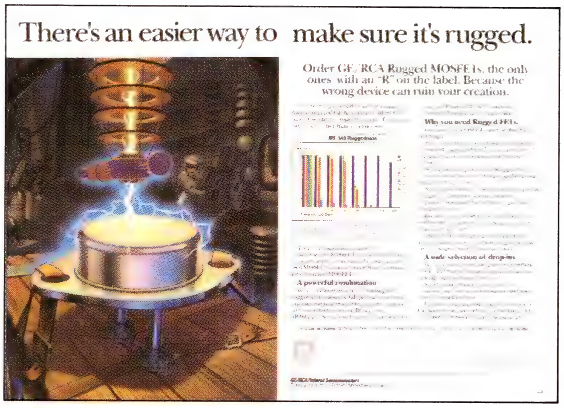
- **COMPANY: Tektronix, Portable Instruments Division**
- **AGENCY: Young & Roehr**
- *"Pictorially inviting and lucid descriptions."*
  Engineering Specialist, Ford Aerospace
- *"Impressive description of superb features."*
  Engineering Test Supervisor, Kepco, Inc.
- *"As always, their ads are detailed without being verbose."*
  Engineer, General Dynamics – Electronics Division.

SECOND RUNNER-UP

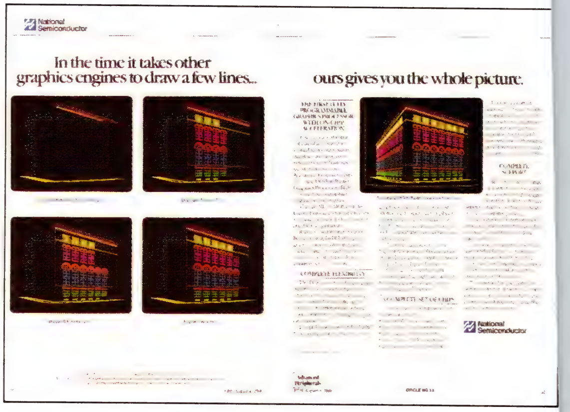
- **COMPANY: GE Solid State**
- **AGENCY: Cappiello & Chabrowe**
- *"Attractive, the type of ad that gets my attention."*
  Senior Associate Principle Engineer, Harris Corporation – GCSD
- *"Impressive. Makes you read on. Excellent ad."*
  Nuclear Electrical Design Engineer, Fairchild Weston/Schlumberger
- *"Colorful pictures. Detailed information on products. Eye-catching."*
  Senior Staff Engineer, GTE Communication Systems

- **COMPANY: 3M, Industrial Chemical Products Division**
- **AGENCY: Kerker & Associates, Inc.**
- *"Not only eye-striking artwork, but also brief, complete information leaving few questions about product and applications."*
  Chief Engineer, Berkshire Technical Devices
- *"Good graphics with excellent detail and text."*
  Project Manager, AMP, Inc.
- *"Interesting lead page develops curiosity about product."*
  Senior Electronic Engineer, Motorola, Inc.

- **COMPANY: GE Solid State**
- **AGENCY: Cappiello & Chabrowe**
- *"Eye-catching graphic, good comparisons."*
  Senior Staff Engineer, Perkin Elmer Corporation/GSS
- *"Eye-catching ad…good layout and text."*
  Test Design Engineer, Dionics
- *"Humorous cartoon, with a good bar chart to get the point across."*
  Senior Manufacturing Engineer, Martin Marietta



- **COMPANY: National Semiconductor Corporation**
- **AGENCY: Foote Cone Belding – Technology Group**
- *"Excellent graphics show their product to be a winner."*
  Electronics Engineer, Naval Research Lab
- *"Eye-catching graphics, appropriate headline, applicable text."*
  Design Engineer, Trans Metrics, Inc.
- *"Clever use of an old phrase. Good presentation."*
  Project Engineer, Martin Decker

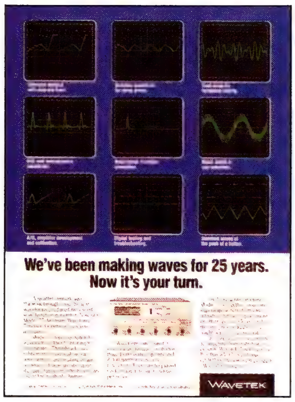


- **COMPANY: Novasenor**
- **AGENCY: Hayes - Rothwell Advertising and Public Relations**
- *"Completely captures one's imagination and the company will be remembered when products are required."*
  Design Engineer, Hewlett-Packard – CSD Division
- *"The graphics catch the eye and the text is well-written and to the point."*
  Product Design Engineer, International Imaging Systems
- *"Reminds me of a vacation. Certainly not the usual, dreary, run-of-the-mill advertisement."*
  Application Engineer, C.E.R.N.

- **COMPANY: Precision Interconnect**
- **AGENCY: Thompson & Huffschmidt**
- *"The obvious is not always easy to achieve...but this ad does it."*
  Engineer, Singer ESDC
- *"Good juxtaposition of concept and example."*
  Design Engineer, Boeing Company BCA
- *"I like the connection between the VW Bug and the baby's legs. A very clever ad."*
  Program Engineer, General Electric

- **COMPANY: SGS-Thomson Microelectronics**
- **AGENCY: Martz & Associates**
- *"Good association between text and picture."*
  Design Engineer, National Semiconductor Corporation
- *"Not only are the colors vibrant, but the ad is informative."*
  Industrial Engineer, Dataproducts New England
- *"Good power of association."*
  Advisory Engineer, IBM General Products Division

- **COMPANY: Wavetek San Diego, Inc.**
- **AGENCY: Chapman/Warwick Advertising**
- *"Ad tells just what the product can do without nonsense or hype."*
  Engineer, Q TRONICS
- *"Performance of instrument is shown clearly in ad."*
  Senior Research Engineer, Infrared Laboratories, Inc.
- *"Waveform photographs get attention and show versatility."*
  Design Engineer, Communications System Specialists



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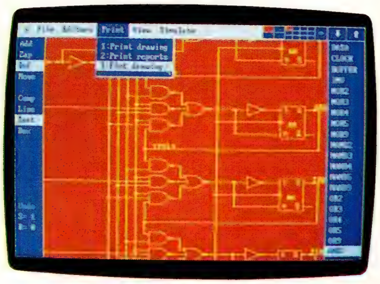

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spectrum

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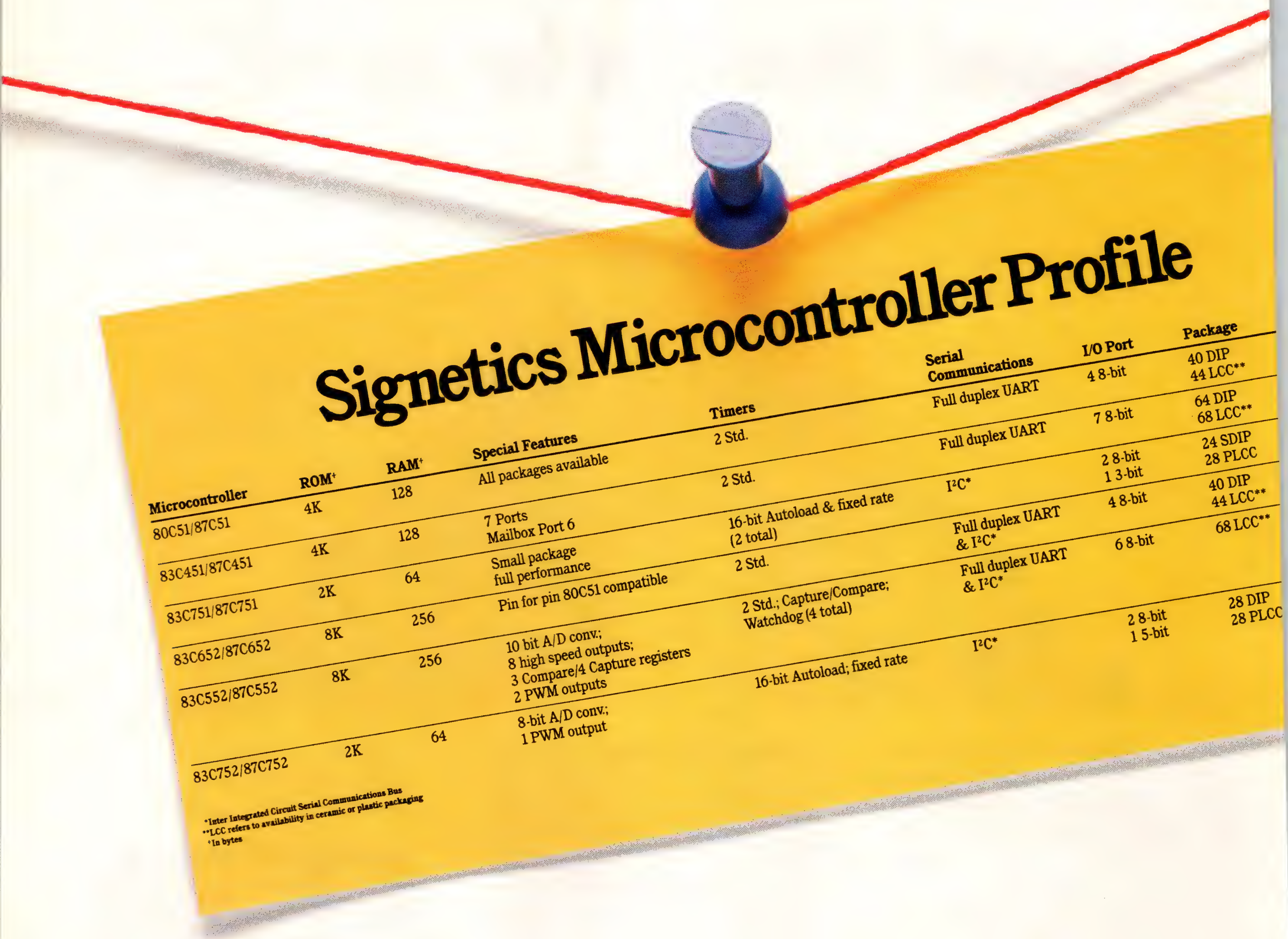

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83C451/87C451	4K	128	7 Ports Mailbox Port 6	2 Std.	Full duplex UART	7 8-bit	64 DIP 68 LCC**
83C751/87C751	2K	64	Small package full performance	16-bit Autoload & fixed rate (2 total)	I^2C*	2 8-bit 1 3-bit	24 SDIP 28 PLCC
83C652/87C652	8K	256	Pin for pin 80C51 compatible	2 Std.	Full duplex UART & I^2C*	4 8-bit	40 DIP 44 LCC**
83C552/87C552	8K	256	10 bit A/D conv.; 8 high speed outputs; 3 Compare/4 Capture registers 2 PWM outputs	2 Std.; Capture/Compare; Watchdog (4 total)	Full duplex UART & I^2C*	6 8-bit	68 LCC**
83C752/87C752	2K	64	8-bit A/D conv.; 1 PWM output	16-bit Autoload; fixed rate	I^2C*	2 8-bit 1 5-bit	28 DIP 28 PLCC

*Inter Integrated Circuit Serial Communications Bus
**LCC refers to availability in ceramic or plastic packaging
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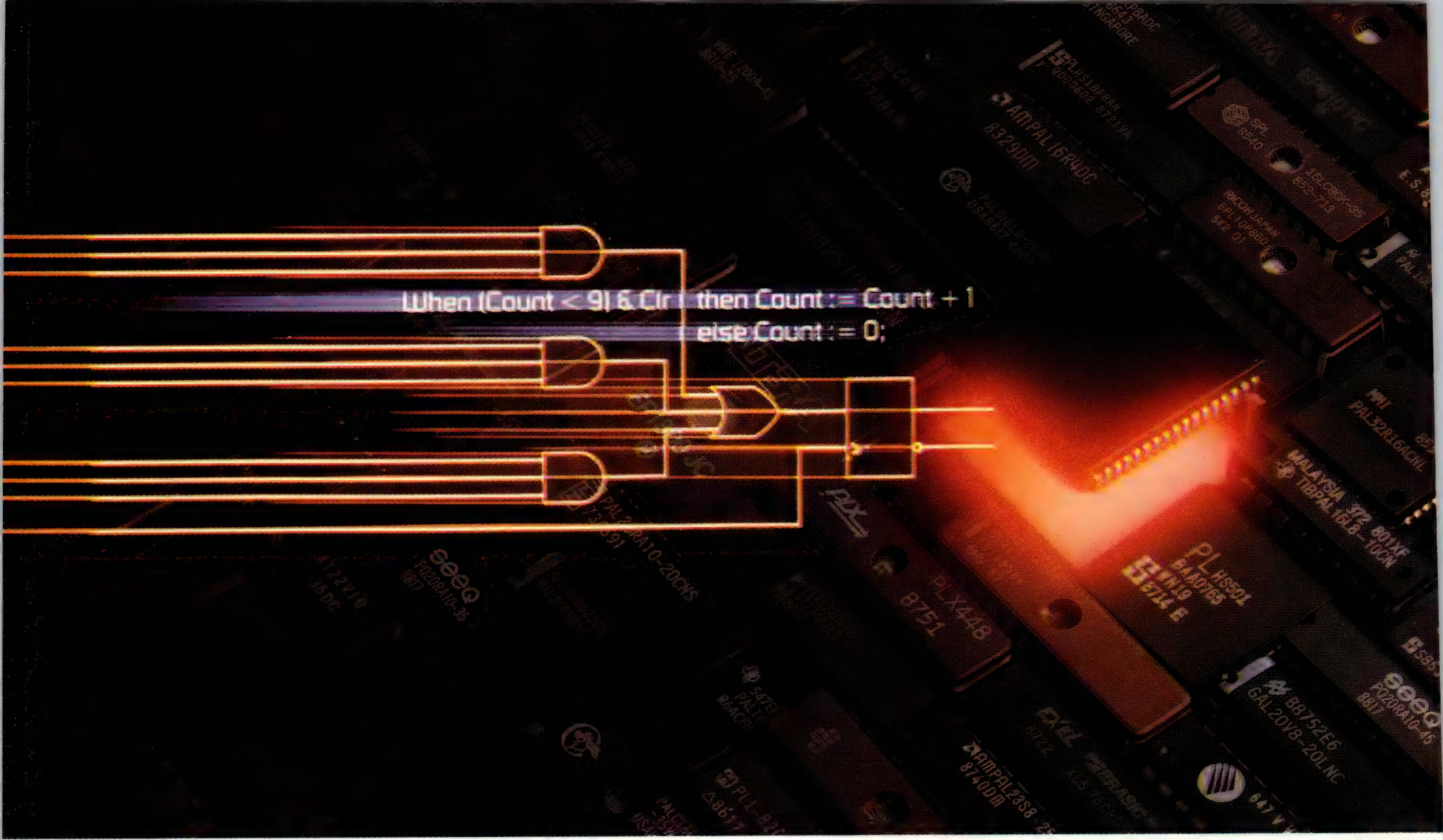

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Check list helps you avoid trouble with PLD designs

Much of the attraction of PLDs is due to their TTL-like nature. However, doing effective system design with these devices requires an extension of TTL system-design techniques

Stan Kopec and Don Faria,
Altera Corp

In the design realm, what you don't know might ultimately hurt the viability of your design. The following list of design tips can help you squeeze more from your PLD logic and avoid common "gotchas" in the development cycle. The majority of the tips are applicable to most PLD types—such as PALs, EPLDs, IFLs, and PLAs—and should be useful no matter what your device preference.

1 High-performance PLDs generate large transient currents during switching. You can help ensure proper operation of the PLDs in your board by liberally using power-supply decoupling capacitors—not using these caps can result in erratic operation, noisy outputs, or total functional failure. Every PLD should have, as a minimum, a 0.1-μF capacitor connected between V_{CC} and ground directly at the device's pins. Some PLD manufacturers recommend larger capacitor values for certain devices, so consult each PLD's data sheet. For devices with multiple V_{CC} pins, decouple each pin separately.

2 Tie all unused input and I/O pins on CMOS PLDs to ground or V_{CC}. Input voltage levels on floating pins can vary from logic 0 to logic 1 levels, causing unused PLD logic to switch unpredictably. This erratic switching can generate additional noise, which affects overall device performance.

3 When your logic requirements exceed the PLD macrocell's supply of product terms, divide the logic network in half, placing each half into a separate macrocell. Then, use one macrocell's feedback line to connect the logic in series. Choose the output nodes of high fan-in OR, XOR, or XNOR functions as logical points for logic partitioning. Note that the ac timing delays for the complete logic network will increase by as much as 80% because of the second macrocell's delay.

4 When close to your limit for PLD power consumption, a few tricks can sometimes save the milliamps you need to meet your power budget. In an all-CMOS circuit path, eliminate unnecessary pullup resistors on device outputs to remove dc current paths. After this step, you'll only have to contend with the ac currents. To minimize dynamic power consumption in the PLD, limit the number of PLD inputs switching at maximum

When close to your limit for PLD power consumption, a few tricks can sometimes save the milliamps you need to meet your power budget.

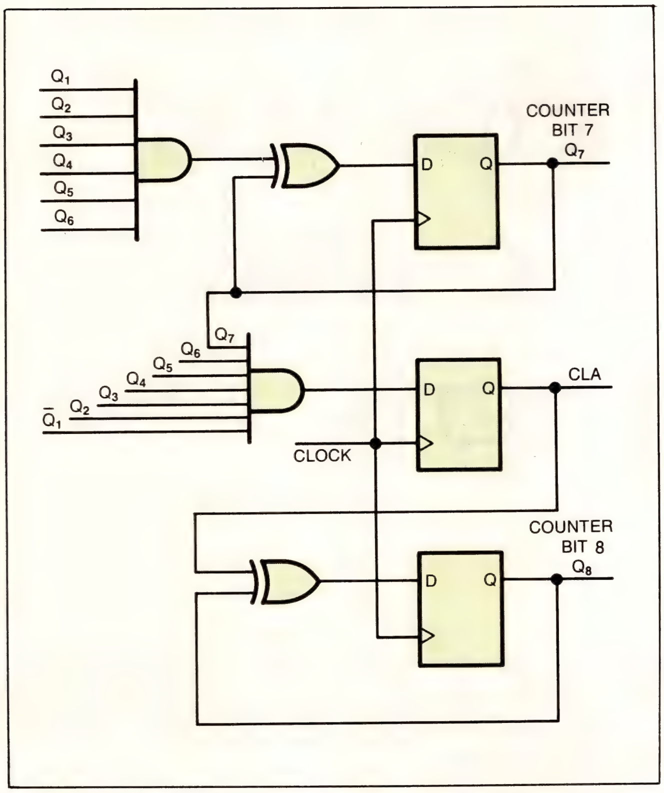


Fig 1—With this carry-look-ahead circuit, *binary counters of 8 bits or more can easily fit within the 8-product-term macrocells offered by most PLDs.*

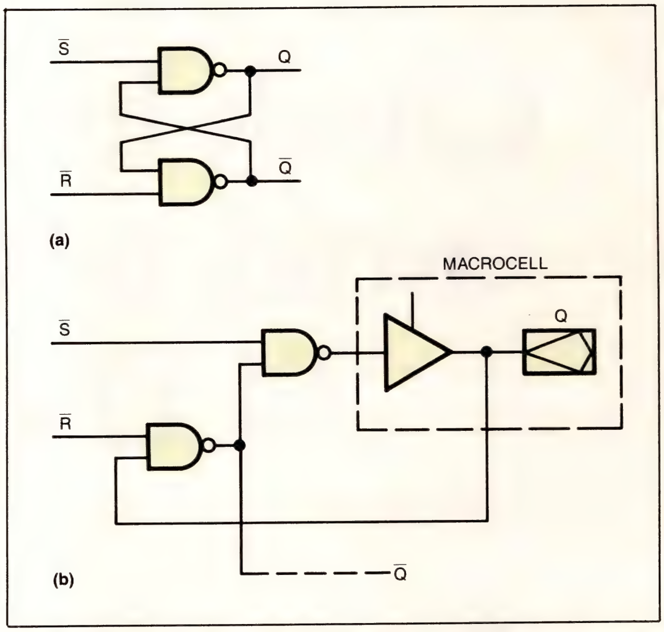


***Fig 2—You can implement asynchronous set-reset latches (a)** in a single macrocell by using combinatorial feedback. The cross-coupled NAND latch in **b** requires one macrocell.*

frequency. Dynamic power consumption is directly proportional to the square of the switching frequency.

5 For large synchronous counters built with D flip-flops, use carry-look-ahead (CLA) circuits when you exceed macrocell product-term limitations. With the CLA circuit in **Fig 1,** binary counters of eight bits or more can easily fit within the 8-product-term macrocells offered by most PLDs. Also, the CLA circuit is synchronized with the counter's clock to avoid any possible glitches. In this example, when the first seven bits of an up-counter reach 1111110, the input to the CLA flip-flop is set high. On the next clock, the seven bits go to 1111111. The CLA output also goes to a 1, toggling the next significant bit of the counter. The CLA output goes low on the following clock cycle.

6 You can build simple and efficient counters with toggle flip-flops. Binary up-counters using T flip-flops require only one product term for each counter bit. The same counter using D flip-flops requires an additional product term for each successive bit. Thus, an 8-bit up-counter requires nine product terms for its most-significant bit when designed with D flip-flops, but only one product term when designed with T flip-flops. Some PLDs offer programmable flip-flops or product-term-controlled XORs, both of which ease the implementation of T flip-flops.

7 You can implement asynchronous set-reset latches in a single macrocell by using combinatorial feedback. The cross-coupled NAND latch in **Fig 2** requires one macrocell. To avoid unwanted output glitches, the input-pulse width must be long enough to allow the input change to propagate through both the macrocell and the feedback structure and return to the NAND gate's input.

8 The registers of some PLDs have asynchronous preset and reset functions. You can use these functions for counter and register preloading, state-machine initialization, and other common logic requirements. But, use with care—because these functions are asynchronous, any input glitches or inadvertent decoding hazards propagate through to the register. You should qualify decoded reset or preset functions with a strobe signal. The strobe signal should go active only after all other asynchronous inputs are stable; it should go inactive before any other input changes.

9 "Buried" logic functions have outputs that get used only within the PLD; consequently, the functions do not require an output pin. When using a macrocell for buried logic, beware of PLDs with only one feedback path into the macrocell's AND-OR array. In these devices, buried logic functions, such as flip-flops in counters or shift registers, also consume the I/O pin. What's more, three-state options for many designs are lost, and you must deliberately "no-connect" the pin at the board. Other PLDs offer a multiplexed feedback path where you may choose feedback before or after the three-state buffer, thus preserving the three-state function. Still other PLDs provide dual feedback, which allows you to bury the macrocell logic while using the I/O pin for an unrelated input. **Fig 3** shows the different types of feedback architectures offered by PLDs.

10 Minimizing PLD switching noise without degrading circuit performance can be a real challenge. A series resistor between the PLD's output and its load can limit ac current and accompanying noise but increase output turn-on times. Or, by clocking logic blocks with both clock edges, you can reduce peak noise because transients are distributed in time. Also, reducing power-supply and wiring inductance also minimizes noise because noise voltage is directly proportional to effective wiring inductance.

11 Driving the I/O pin above V_{CC} or below ground can result in latch-up on CMOS PLD I/O pins. Latch-up occurs when the parasitic bipolar transistors invariably present in all CMOS devices fire in an SCR-like action. If you limit input signal excursions to 500 mV outside of each rail, you can usually avoid the problem. You should take particular care to ensure that the input signals' turn-on does not lead the supply's turn-on during system and device power-up. In extreme cases, you can prevent latch-up by inserting series resistors between the device pin and its signal source. Even resistors of 100Ω can materially improve the situation because voltage and current injected into the I/O pin must exceed device-specific levels to trigger the parasitic SCR.

12 When you reuse a UV-erasable programmable logic device (EPLD) be sure to follow the manufacturer's recommendations on erasure time and dose. Devices may sometimes verify as blank in the PLD programmer, yet be only partially erased. The

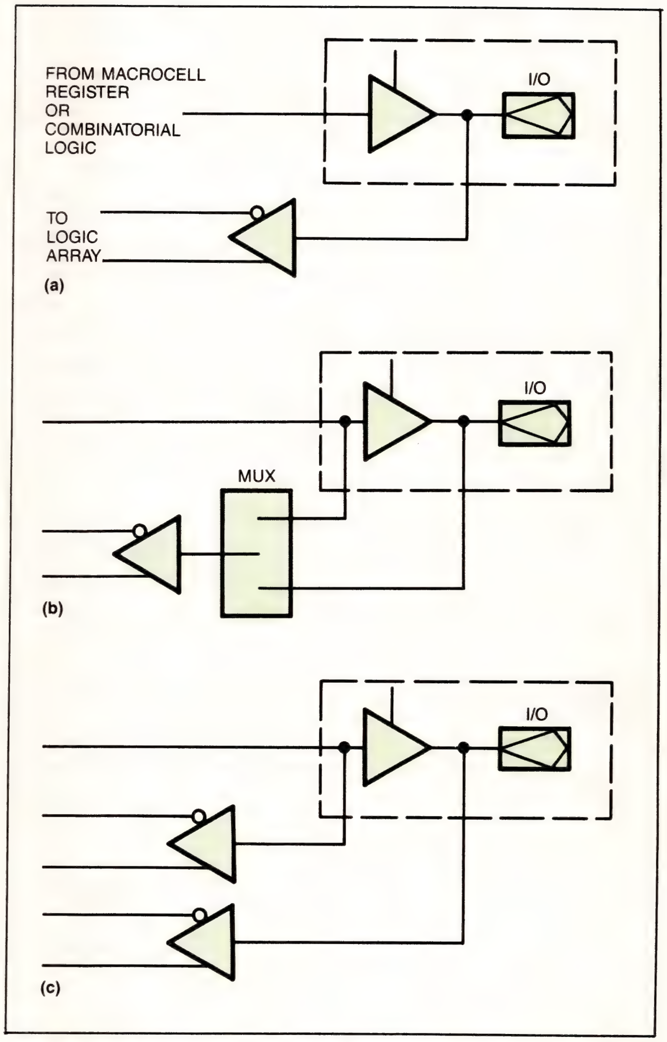


Fig 3—When using a macrocell for buried logic, *beware of PLDs that have only one feedback path into the macrocell's AND-OR array* ***(a)****. In these devices, buried logic functions, such as flip-flops in counters or shift registers, also consume the I/O pin. Other PLDs offer a multiplexed feedback path* ***(b)*** *or dual feedback* ***(c)****, which allows you to bury the macrocell logic while still using the I/O pin for an unrelated input.*

result can be degraded ac performance after reprogramming, or outright functional failures. When erasing large quantities of EPLDs, do not overload the eraser—devices on the periphery of the tray may be too far from the UV-light source to fully erase, even after the recommended interval.

13 Build timing margins into your system to provide a guardband against PLD delay skews. Skews between parallel paths of logic are inherent in PLD structures. Propagation delays between macro-

Some PLDs offer programmable flip-flops or product-term controlled XORs, both of which ease the implementation of T flip-flops.

cells can vary by as much as five percent on supposedly parallel paths. Maximum combinatorial delays are guaranteed by the manufacturer, but delay matching is not. Minimum delays can vary from vendor to vendor, and they also depend on the speed grades of the device.

14 You must conform to PLD input rise- and fall-time specifications for proper operation. If the input rise or fall time is too slow, noise or stray feedback can cause multiple transitions when the input voltage is near the threshold of the input stage. These multiple transitions can lead to output glitches or internal oscillation. Use external Schmitt triggers to condition the PLD's inputs to correct for slow rise- and fall-time signals.

15 You can easily emulate J-K or T flip-flops with a D flip-flop and feedback as in **Fig 4**. These flip-flops provide alternative solutions to sequential logic designs such as state machines and counters.

16 Address-decoder product-term consumption is not only a function of the size of the decoded address range but also is a function of the base, or starting address, of the block. If the block of addresses is of size 2^N, where N is a non-negative integer, and the starting address of the block is on a 2^N (or multiple thereof) boundary, you can implement the decoder with a single product term **(Fig 5)**. In such a situation, you specify the low-order N bits of the address as "don't care" to give the correct product-term expression. If such decoder assignments make sense for your system, use them; the fewer product terms required, the wider the range of PLDs that will work. For example, the block 4 through 7_{HEX} takes a single product term:

$$A3'*A2,$$

which is one product term of size 1.

If a decoded address range is of size 2^N but not on a 2^N boundary, you must OR multiple product terms in order to get the correct decoder function. In this case, the design method is to piece together the overall function, starting with the largest block that is a power of 2 within the overall range and adding progressively smaller product terms to cover the whole range. For example, to decode addresses 9 through C_{HEX} assuming four address inputs, the terms would consist of

$$A3*A2'*A1 + A3*A2'*A1'*A0 + A3*A2*A1'*A0'.$$

These product terms cover address blocks of size 2, 1, and 1.

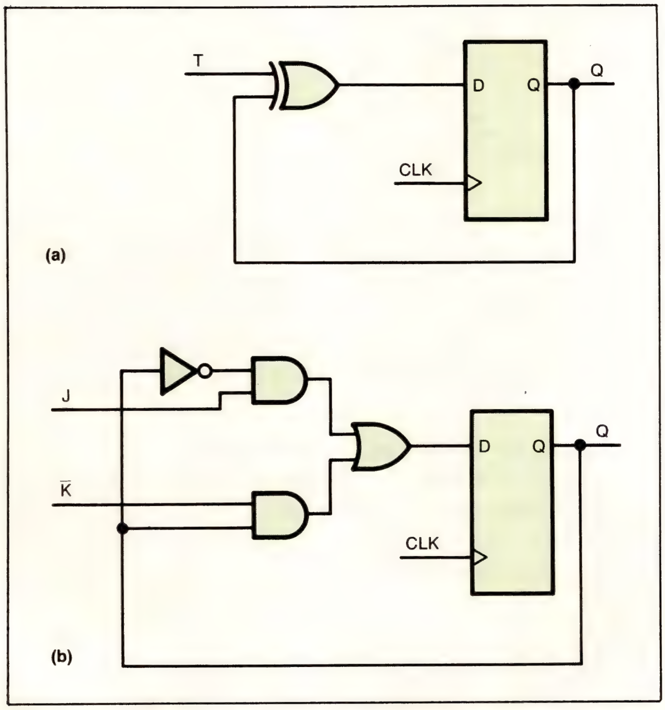


***Fig 4—You can use D flip-flops to emulate** both T flip-flops **(a)** and J-K flip-flops **(b)**.*

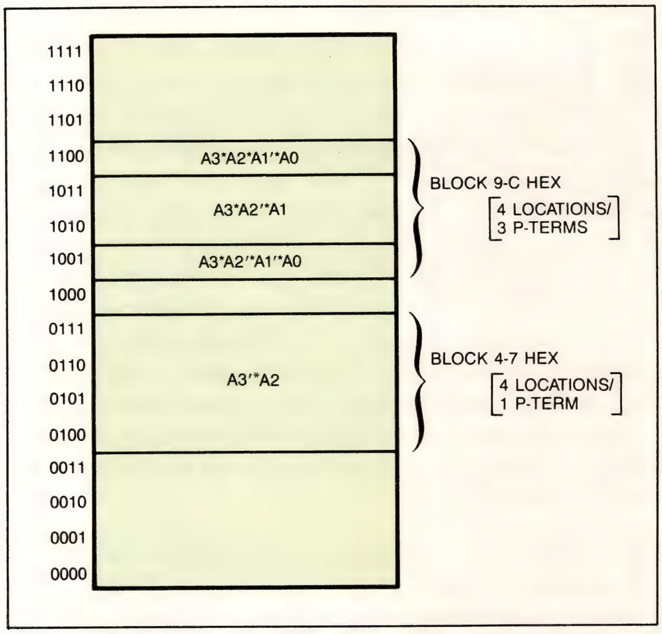


***Fig 5—Product-term consumption** varies with block size and base address.*

17 You should rigorously observe PLD power-supply maximum rise-time specifications. Generally, the slower your power supply's turn-on, the more room for problems. Many new PLDs perform power-on-reset of registers or load device-configuration data during power-up. In some PLDs, on-chip power-supply voltage monitors trigger these functions during power-up. Slow slew rates open the door for noise problems and other gremlins associated with these circuits.

18 Logic functions such as parity checkers, adders, and comparators make extensive use of the exclusive-OR (XOR) function. When implementing any XOR function, beware of the rapid consumption of product terms that can result from their use. The basic 2-input XOR function requires two product terms. Cascading XOR gates N levels deep results in a minimum requirement of 2^N product terms. Given an eight product-term macrocell in a standard PLD, you can fit, at best, a 4-bit parity checker into a single-level macrocell. PLDs with XOR gates built into their macrocells can alleviate the problem and let you pack more of such logic into a single level.

19 When designing with PLDs, the specification for gate delay is unimportant. PLDs contain AND-OR logic arrays that implement all combinatorial logic; and AND-OR arrays have fixed delays, which are independent of the number of gates implemented. PLD design software typically removes redundant logic in your design. Consequently, chaining gates together to add delay elements, such as inverters, does not add logic delay. If you need to add delay elements, you must partition the logic across macrocells connected in series.

20 You can emulate open-drain and open-collector outputs in your PLD with three-state outputs. Open-drain and -collector outputs produce either a logic 0 or a high-impedence state. By driving the data input of the three-state buffer with a fixed logic 0 and using the PLD's output-enable product term for logic control, you can emulate open-drain outputs **(Fig 6)**. For such outputs, match the PLD's I_{OL} (current-sinking) specifications and pullup resistor values to ensure proper V_{OL} levels.

21 Most CMOS PLDs function correctly when driven with either TTL- or CMOS-level inputs. If you use TTL levels, the input stages on the PLD

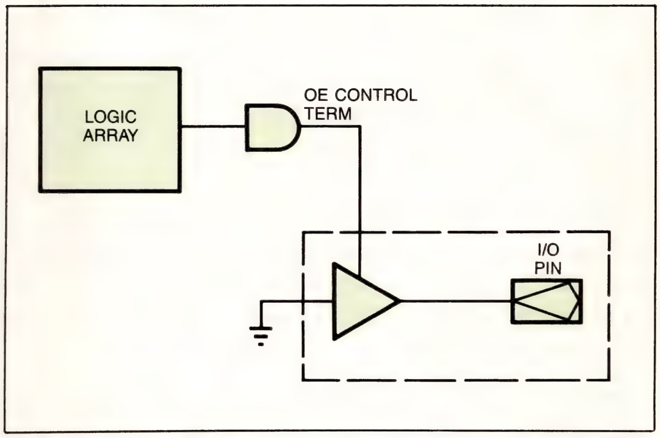


***Fig 6—By driving the data input of the three-state buffer** with a fixed logic 0 and using the PLD's output-enable product term for logic control, you can emulate open-drain outputs.*

may require additional dc. To minimize power consumption, however, use input levels as close to the supply rails as possible. Pullup resistors can assist full switching when TTL outputs drive the device.

22 You can double the output drive of your PLD by connecting output pins together. Each internal macrocell must implement the same logic function; that is, each must be programmed identically. Be sure to have decoupling capacitors connected between V_{CC} and ground at the chip to eliminate switching noise.

23 If incorrectly handled, asynchronous inputs can cause a variety of problems in PLD-based circuits. Metastability problems occur when asynchronous inputs cause clocked registers to behave in an analog, or non-digital, manner during operation. To avoid such problems, synchronize inputs to the destination logic's clock prior to actual use. Connect the asynchronous input to the D input of an edge-triggered flip-flop, clock the flip-flop with the clock of the PLD logic, and then use the flip-flop's output as a synchronized version of the original input. You can implement this scheme in dedicated edge-triggered registers, such as the 7474 and 74374, or use a PLD macrocell's register to perform the synchronization for the logic in the remaining macrocells.

24 The benefits of surface-mount packaging, such as plastic leaded chip carriers, are well known. The key points behind its growing popularity are smaller pc-board footprints than DIPs and better ac performance because of lower lead inductance. How-

Minimizing PLD switching noise without degrading circuit performance can be a real challenge.

ever, during prototyping and in production situations where surface-mounted devices are socketed, beware! The small size and large number of leads typical of these devices make reliable socketing more difficult than with DIPs. In addition, package dimensions may vary slightly from manufacturer to manufacturer, so sockets may not provide proper contact force and alignment for all devices. Always use sockets recommended by the PLD manufacturer for their specific devices; all "standard" sockets are not the same.

25 Watch out for monostable multivibrators and RC oscillators built with PLDs; their duty cycles depend on the input threshold of the specific PLD used. Because the exact threshold of input transistors varies for each device, so does the duty cycle. Choose resistor and capacitor values to meet your timing requirements, but do not exceed the timing specifications of the PLD. For more precise timing, use a quartz crystal in conjuction with the PLD (**Fig 7**).

26 Although there are many PLD programmers available, not all of them have been evaluated by each PLD manufacturer for proper programming yields and adherence to the manufacturer's recommended programming algorithms. You should always check with the PLD manufacturer to see if it has evaluated a given programmer for a specific device. You should also frequently calibrate your programmer. Programming PLDs with equipment that is not compliant with the PLD manufacturer's specifications can result in poor programming yield, functional failure, or intermittent in-system device operation. A call to the PLD manufacturer's applications group can save you time and money.

27 The difference between maximum flip-flop toggle rates and the true operating frequency of your PLD can be significant. Check the ac specifications from each manufacturer to determine its definition of maximum clock frequency (f_{MAX}). Some f_{MAX} values merely represent pipeline-data toggle rates; others represent maximum operating frequency when implementing sequential functions, such as counters.

28 Two PLDs with the same part number from two different manufacturers will typically *not* use the same programming algorithm. One reason for

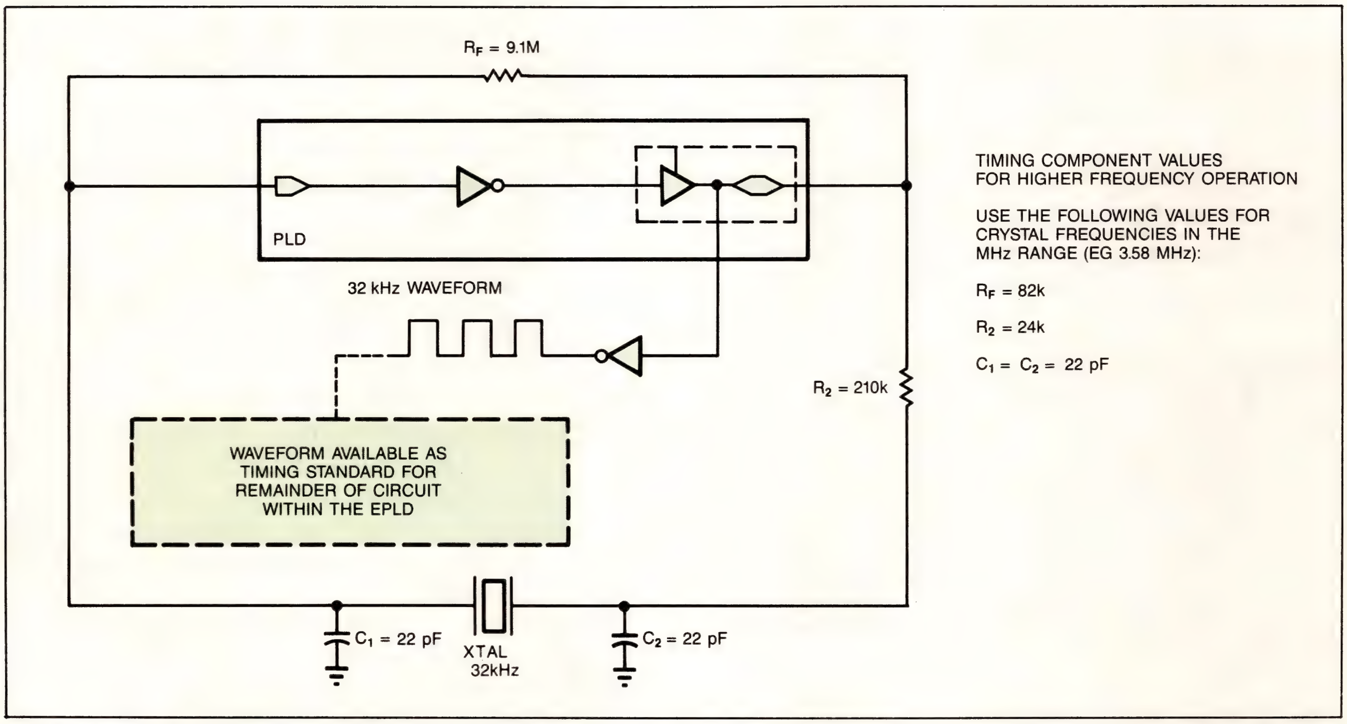


Fig 7—For timing more precise than that you can achieve *using monostable multivibrators and RC oscillators built with PLDs, use a quartz crystal in conjuction with the PLD.*

this difference is that although devices may be functionally equivalent, they may use different programmable-link technologies, such as fuse, antifuse, EPROM, and EEPROM. Always set up your PLD programmer for the correct device type *and* device manufacturer before programming the part.

29 PAL (programmable-AND/fixed-OR) or PLA (programmable-AND/programmable-OR) device architectures: which is better? Up front, PLAs sound more flexible. PLAs let you assign as many product terms as you need (within device limits) to a single logic function. This flexibility can assist in generating product-term-rich functions. However, the added programmable array means lower operating speeds; and the total number of registers and product terms available on PLA chips generally is lower than fixed-OR PLDs. Practically speaking, PLAs get used sparingly because of their cost, performance, and capacity limitations.

30 Security bits ensure the safety of your designs after your PLDs have gone into production by disabling the program-read or -verify function. But take care not to program the security bit too early. Once you program the security bit, you cannot update one-time-programmable (OTP) PLDs with design patches. However, you can sometimes turn OTP PLDs programmed with source design errors from expensive mistakes into working components by programming additional bits the second time around.

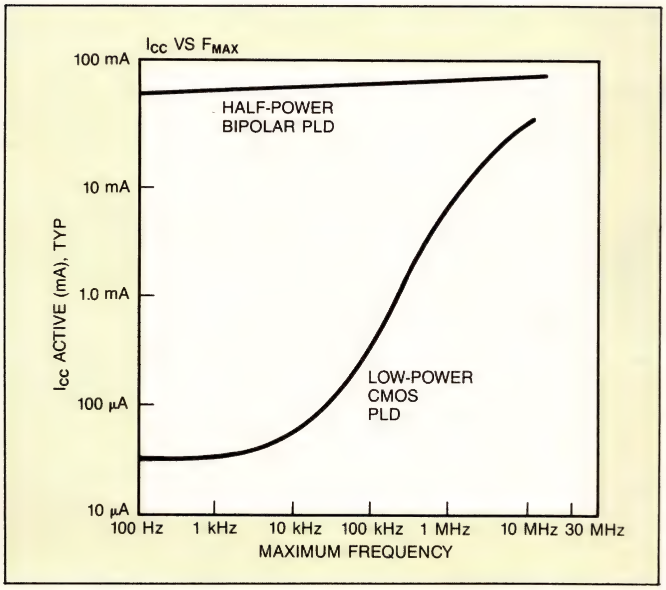


***Fig 8—The power-vs-frequency characteristics of CMOS** and bipolar PLDs are inherently different.*

31 The power-vs-frequency characteristics of CMOS and bipolar PLDs are inherently different (**Fig 8**). Bipolar PLDs have a relatively flat current-vs-frequency curve; standard PALs consume 180 mA at 10 kHz or 10 MHz. CMOS PLDs typically require lower currents at low frequencies (tens of microamps to tens of milliamps) but may exhibit an increase in supply current to levels approaching those of bipolar devices at high frequency. Always consult device data sheets for expected currents at the operating frequency of the PLD—not necessarily the overall system clock rate.

32 PLDs with grouped control functions can restrict your design options. Grouped control means a single signal affects all registers or macrocells in a group or PLD. Many of the latest PLDs provide separate product terms for clock, clear, preset, and output-enable control, thereby allowing independent control of each macrocell.

33 When interfacing TTL outputs with CMOS-PLD inputs, check to see if your PLD's inputs are TTL-compatible. If not, you have to connect a pullup resistor at the TTL output to match the input voltage (V_{IH}) of your PLD. Choose a resistor value R, where $R = V_{CC} - 0.4/I_{OL}$ of the TTL device.

34 High-density PLDs frequently have more than one ground pin or lead—but don't take any of them for granted. You must tie all ground pins or leads to the pc board's ground plane directly at the device. Careless board layout can introduce excessive inductance in a ground lead. The result can be incorrect PLD operation because of noise.

35 Cover windows on UV-erasable PLDs with opaque labels. Constant exposure to room-level fluorescent lighting erases an EPLD in approximately three years. Erasure takes only a week if the EPLD is exposed to direct sunlight.

36 When implementing a PLD design, look at ways to use the combinatorial logic horsepower in the chips fully. Avoid unnecessarily decoding signals used by your PLDs. A PLD's product terms

Skews between parallel paths of logic are inherent in PLD structures.

decode input variables nicely. Presenting to the PLD two inputs that encode four values saves pins compared to four distinct inputs and can give better overall system performance.

37 When designing state machines, determine if your PLD provides a power-on reset feature. If it does, all registers initialize to a logic 0 upon power-up. The first state in your PLD's state-machine design file must correspond to this initialized state (all state variables set to 0). State-transition specifications from the power-up state can then be either conditional (dependent on inputs) or unconditional (independent of inputs).

38 Some PLDs offer you the option of clocking macrocell registers from either a dedicated clock input or a clock product term from the logic array. Clocking registers with a product term results in longer clock-to-output delays because of the added programmable-array delay. But, on the positive side, you can generate a unique clock function for each macrocell. For minimum skews, however, you should clock the registers with the dedicated input.

39 PLDs frequently have an external feedback path from the macrocell I/O pin as well as from the internal-register output (**Fig 9**). Delays are greater with the pin feedback path than with the internal feedback path. For maximum logic clock rates, use the internal feedback path whenever possible. Typically, if you are not using the macrocell's output externally to the PLD, you can use internal feedback.

40 When your PLD design is ready for production, you have two routes you can take to reduce costs. If you start with EPLDs, some manufacturers offer one-time-programmable parts at reduced cost. With a fuse-based design, some manufacturers offer mask-programmed devices—in effect a small gate array. But, be aware that mask-programmed devices incur production lead-time and development charges.

41 Does your design need a multiplexer? A good rule-of-thumb is that an N-input multiplexer requires N product terms. Thus, an 8:1 multiplexer fits nicely into an 8-product-term macrocell.

42 Many PLDs provide programmable macrocell-output inversion. This inversion feature, usually controlled by an XOR gate, provides the option of implementing either active-high or -low logic. PLD software packages that provide automatic logic-minimization algorithms can utilize DeMorgan's inversion to reduce the total number of product terms required to realize a design.

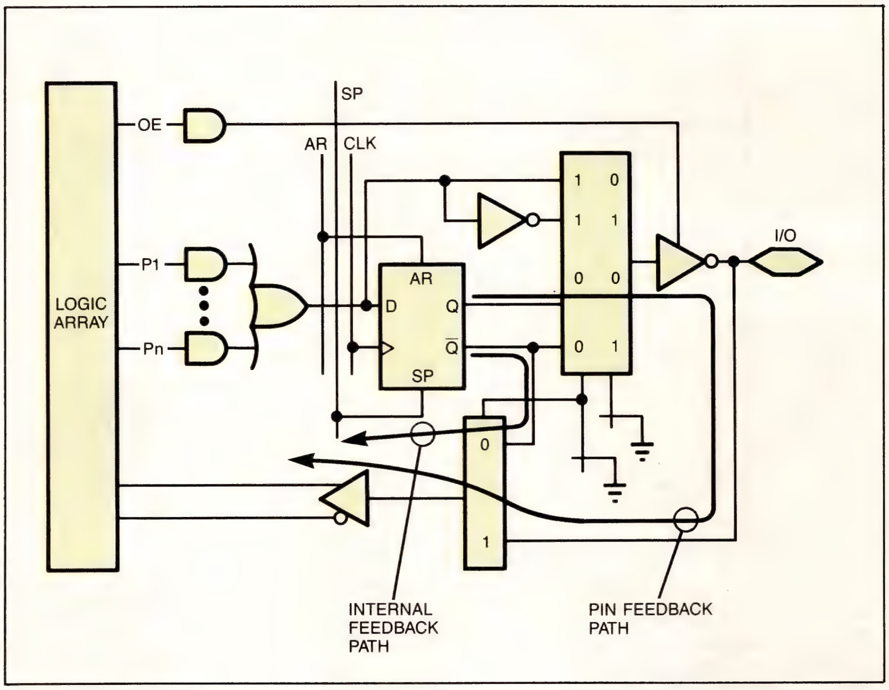


Fig 9—PLDs frequently have an external feedback path *from the macrocell I/O pin as well as from the internal register's output.*

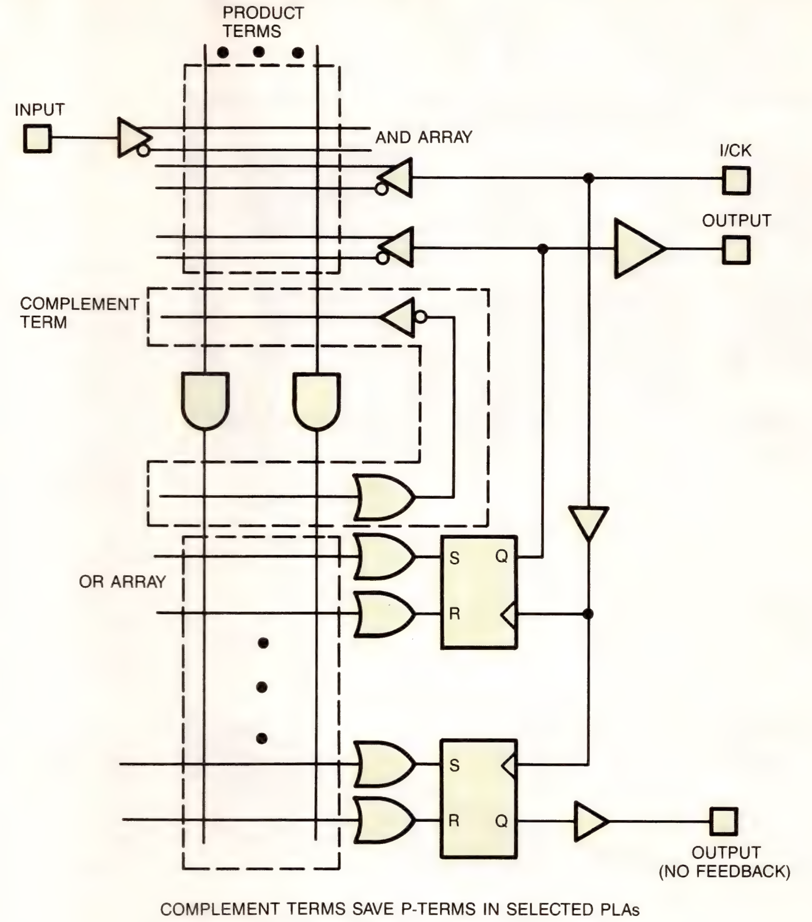


***Fig 10—Certain PLAs have complement terms** or even a complement array. You can use the complement features for creating "default" logic expressions—explicit expressions specifing what must happen if none of the expected inputs are true.*

43 Certain PLAs have complement terms or even a complement array **(Fig 10)**. Both consist of an inverting OR term that feeds directly back into the AND plane of the chip. You can use the complement features for creating "default" logic expressions—explicit expressions specifying what must happen if none of the expected inputs are true:

IF .NOT. A .AND. .NOT. B .AND. .NOT. C
THEN . . .

where A, B, and C are the outputs of product terms from the AND array. This structure is particularly useful in state-machine designs, where default-state, or hold-state, transitions often occur.

44 Don't exceed the absolute maximum ratings of PLDs. Operating devices above the maximum specifications listed by the manufacturer may cause them permanent damage. These specs are only stress ratings of the device and do not imply that you can actually operate the devices at these conditions or any conditions above those indicated in the operational section. Exposure to the absolute maximum stress ratings for extended periods of time can affect a device's reliability. Most PLDs, even CMOS ones, are specified only for standard TTL supply voltages: 5V ± 5%. Extended operating voltages tolerated by SSI CMOS logic (2 to 6V) are, in general, not appropriate for CMOS PLDs.

45 Using a handler for the production programming of PLDs can be tricky. Even with an adequate programmer, the extra cabling inductance can cause programming difficulties at the handler contacts, and voltage and timing relationships can be dramatically distorted at the device. Always consult the programmer and PLD manufacturers for information on a handler interfacing before the fact—you will save time and money.

46 Do you have a "simple" PLD design change and feel tempted to edit the JEDEC programming file directly instead of recompiling the design from scratch? A word of caution: Don't. Editing JEDEC maps is error-prone and results in devices whose operation is inconsistent with source documentation. Whatever design entry form you use, recompiling is more accurate and will ultimately save you hassle.

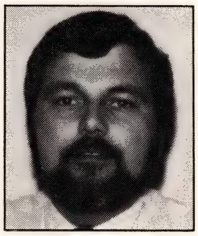
47 When interfacing PLDs to high-performance buses, note whether your PLD provides a fast output-enable/disable option. PLDs with this capability provide a direct connection from a dedicated input to

the three-state buffer. Some PLDs offer a programmable option allowing the output-enable function to be controlled directly either by a dedicated input or by a product term.

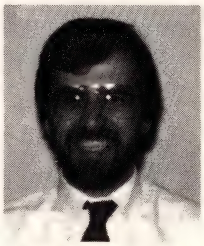
48 Observe electrostatic discharge precautions with both bipolar and CMOS PLDs. Although these devices contain circuitry to protect inputs from high static voltages and electric fields, make sure that you are properly grounded before handling the devices. Follow proper pc-board design practices to avoid applying any ac or dc voltage that is outside a PLD's absolute maximum rated voltage.

49 When prototyping with modern high-performance PLDs, don't get sloppy. Intermittent, hair-pulling operation can be the result. Use multilayer boards with integral ground and supply planes, even at the wirewrap stage; keep wire lengths to a minimum; bypass all devices, PLD and non-PLD alike, on the board; and use high-quality sockets and edge connectors.

Authors' biographies



Stan Kopec is the strategic marketing manager for Altera Corp, where he has been employed for $3^1/_2$ years. Previously, he did IC design and planning for EXEL, SEEQ, and Intel. Stan has a BSEE from the State University of New York at Buffalo and an MSEE from the University of Illinois. He also has two patents pending. In his spare time, he enjoys skiing, golfing, and raquetball.



Don Faria defines the architecture for new products as the product-planning manager at Altera Corp. He has been with Altera for four years and previously worked for Hewlett-Packard. Don has a BSEE from the University of Massachusetts. In his spare time, he enjoys both water and snow skiing and white water rafting.

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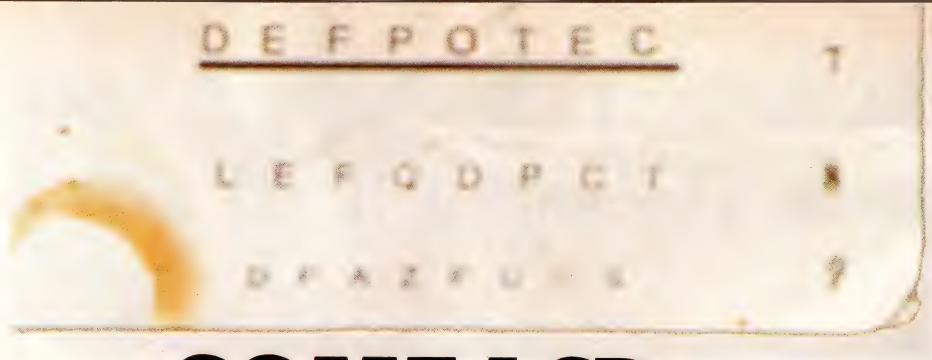

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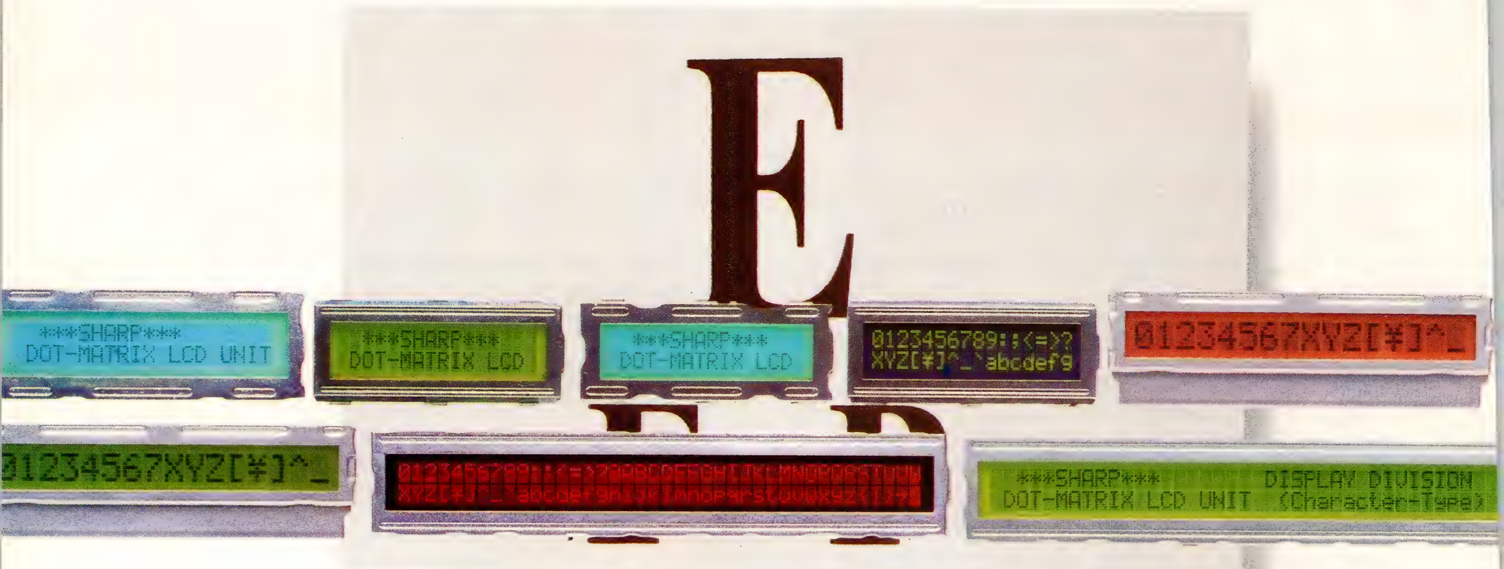

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CIRCLE NO 61

DESIGNER'S GUIDE

dc/dc converters
Part 4

Switched-capacitor networks simplify dc/dc-converter designs

This article, part 4 of a 4-part series, shows how to use switched-capacitor networks to replace inductors in dc/dc converters. Parts 1 through 3 of the series discussed the design of 5 to ±15V converters, the criteria for selecting proper instrumentation for converter design, and the design of power-conservative converters.

Jim Williams and Brian Huffman,
Linear Technology Corp

The inductor, a key component in a typical dc/dc converter, can negatively affect converter design and operation. The most common problem the inductor causes is saturation, a condition that can often result in destructive failure of the converter. The inductor also adds a number of negative factors to your design considerations—it's expensive, relatively large, and can be scarce, and it also has heat-related problems. Fortunately, you can sometimes replace the inductor without affecting your converter's performance. One way is to use a switched-capacitor network as an energy-storage element. Such a network can significantly simplify the dc/dc-converter-design process.

Back to basics

To understand the theory of switched-capacitor converter operation, it might help to review how a basic switched-capacitor building block **(Fig 1)** functions. In **Fig 1a,** C_1 charges to V_1 when the switch is in the left position. The total charge (q_1) on C_1 equals C_1V_1. When the switch moves to the right position, C_1 discharges to voltage V_2. The total charge (q_2) on C_1 will now equal C_1V_2.

Note that the switch action has transferred charge from the source (V_1) to the output (V_2). The total charge is:

$$q = q_1 - q_2 = C_1(V_1 - V_2).$$

If you cycle the switch f times per second, the charge transfer per unit time (current) is:

$$1 = fq = fC_1(V_1 - V_2).$$

If you rewrite this equation in terms of voltage and equivalent impedance, you wind up with an equivalent resistance for the switched-capacitor network:

$$1 = \frac{V_1 - V_2}{\frac{1}{fC_1}} = \frac{V_1 - V_2}{R_{EQUIV}}.$$

The new variable R_{EQUIV} is equal to $1/fC_1$.

Switched-capacitor converters such as the LT1054 have the same switching action as the basic switched-capacitor building block. Although the preceding simplified analysis doesn't consider parameters such as finite switch on-resistance and output-voltage ripple, it does provide an intuitive feel for how the device

Converters such as the LT1054 have the same switching action as does the basic switched-capacitor building block.

works. For example, the analysis explains voltage loss as a function of frequency. As frequency decreases, the $1/fC_1$ term will eventually dominate the output-impedance figure, and voltage losses will rise.

Note that losses also rise as frequency increases, because of internal switching losses resulting from the loss of some finite charge on each switching cycle. When multiplied by the switching frequency, this charge loss per unit cycle becomes a current loss. This loss is particularly significant at high frequencies.

The oscillators in practical converters are designed to run in a frequency band that will minimize these losses. **Fig 1c** is the block diagram of the LT1054. The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter and regulator. Its adaptive drive scheme optimizes its efficiency over a wide range of output currents. Its total voltage loss at a 100-mA output current is typically 1.1V. This loss figure holds true over the full supply-voltage range of 3.5 to 15V. The part's quiescent-current drain is typically 2.5 mA.

When you combine it with an external resistive divider, the LT1054 provides a regulated output, which will withstand changes in input voltage and output current. The LT1054 can operate in a standby mode—at a quiescent current of only 100 μA—when you ground the feedback pin. The internal oscillator runs at a nominal frequency of 25 kHz. You can use the oscillator pin to externally adjust the oscillator frequency or to synchronize the LT1054's operation.

Getting rid of inductors

Most converters employ inductors simply because inductors can store energy. This stored magnetic energy, released and expressed in electrical terms, is the basis of dc/dc-converter operation. Inductors are not the only components that can store and efficiently release energy, however. Capacitors can store energy; thus, they can serve as the basic transfer element in dc/dc-conversion processes.

Fig 2a illustrates the inherent simplicity of a switched-capacitor-based dc/dc converter. The LT1054 provides clocked drive to charge C_1. A second clock

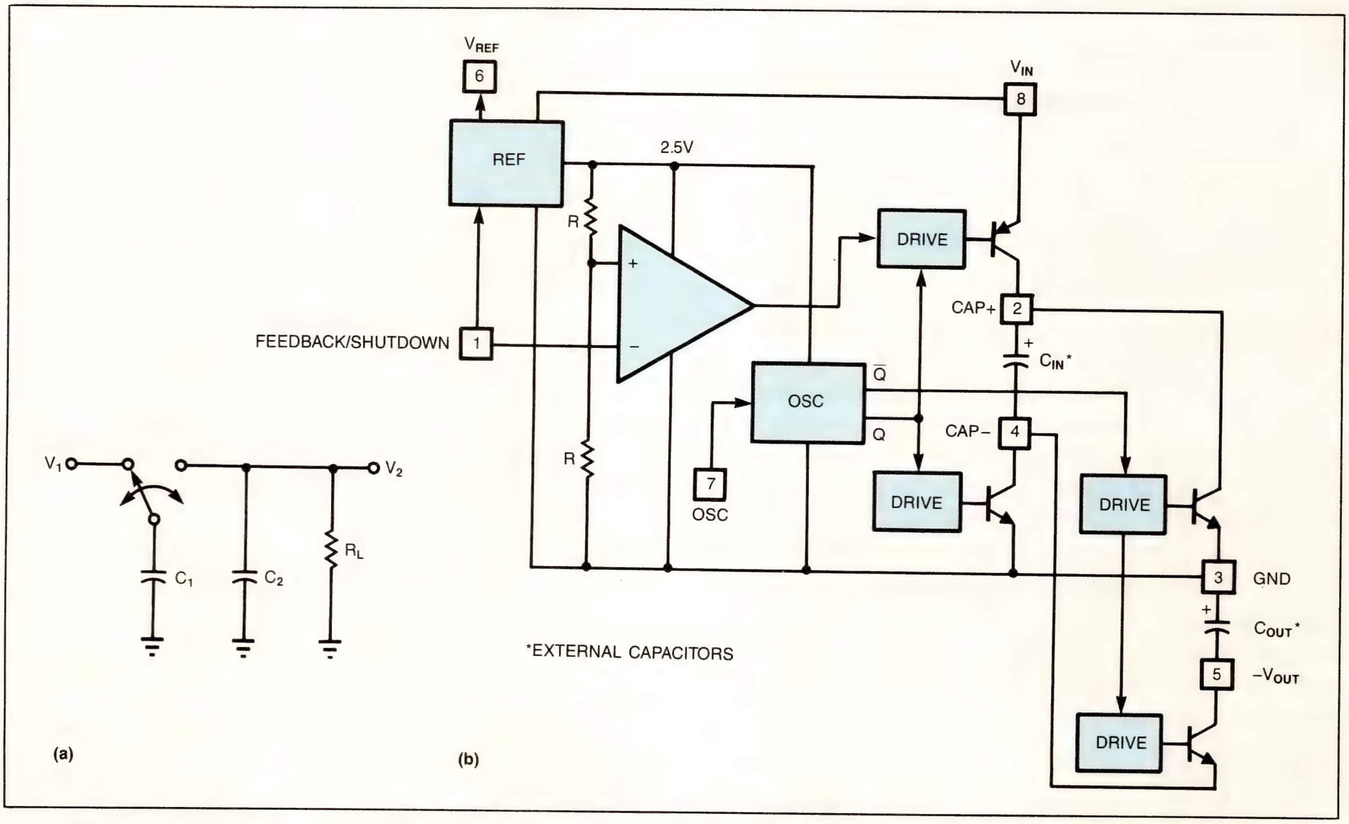


Fig 1—When the switch is in the left position, *the total charge on C_1 in a basic switched-capacitor building block **(a)** equals C_1V_1. When the switch moves to the right position, C_1 discharges to voltage V_2 and total charge on C_1 now equals C_1V_2. Switched-capacitor converters like the LT1054 **(b)** have the same switching action as the basic switched-capacitor building block.*

phase discharges C_1 into C_2. The internal switching scheme is designed to flip C_1 during the discharge interval and produce a negative output at C_2. Continuous clocking allows C_2 to charge to the same absolute level as that of C_1. Junction losses and other losses preclude ideal results, but the circuit's performance is quite good. **Fig 2b** shows how well the circuit converts V_{IN} to $-V_{OUT}$.

By adding some external steering diodes, you can alter **Fig 2**'s circuit to develop a design that converts a negative input to a positive output **(Fig 3a)**. By modifying the circuit somewhat, you can develop a converter **(Fig 3b)** that transforms a 6V input into ±5V outputs. **Fig 3b**'s circuit is extremely flexible. If you provide some diode steering, the circuit will provide some voltage boost and develop an output of approximately $2 \times V_{IN}$.

Satisfying high power needs

By employing some discrete devices, the switched-capacitor converter in **Fig 4** can provide a 5W output (5V at 1A). The LTC1043 switched-capacitor building block provides nonoverlapping complementary drive to the four MOSFETs. The MOSFETs are arranged so that C_1 and C_2 are alternately in a series and a parallel configuration.

During the series phase, the 12V supply current

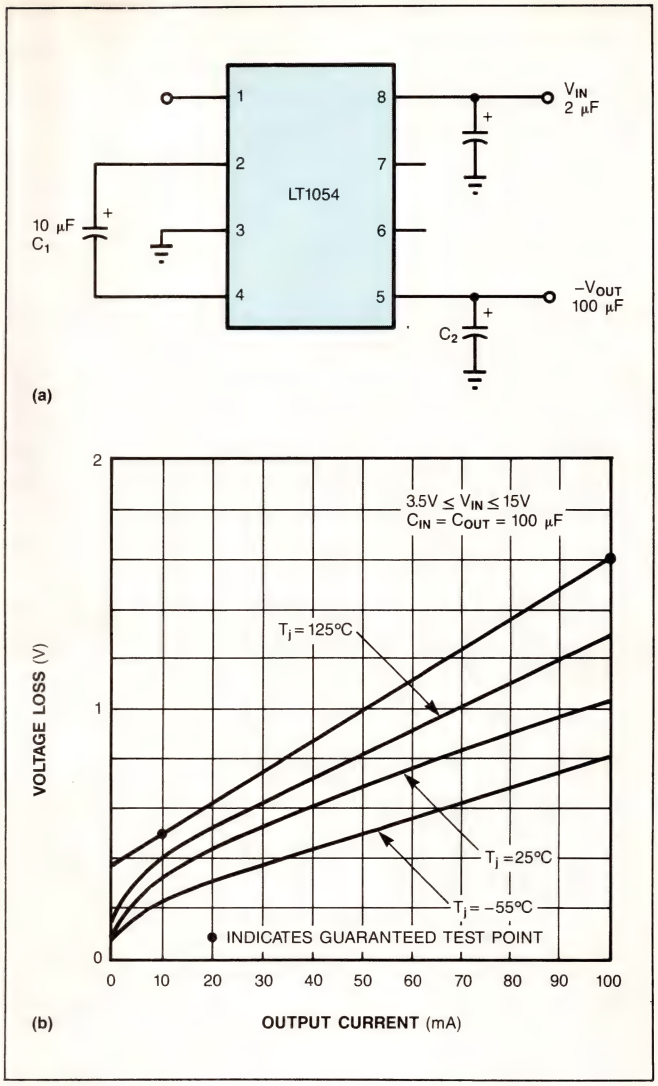


*Fig 2—**Circuit simplicity is an inherent feature** of a switched-capacitor based dc/dc converter **(a)**. Despite its simplicity, this circuit does a good job of converting V_{IN} to $-V_{OUT}$ **(b)**.*

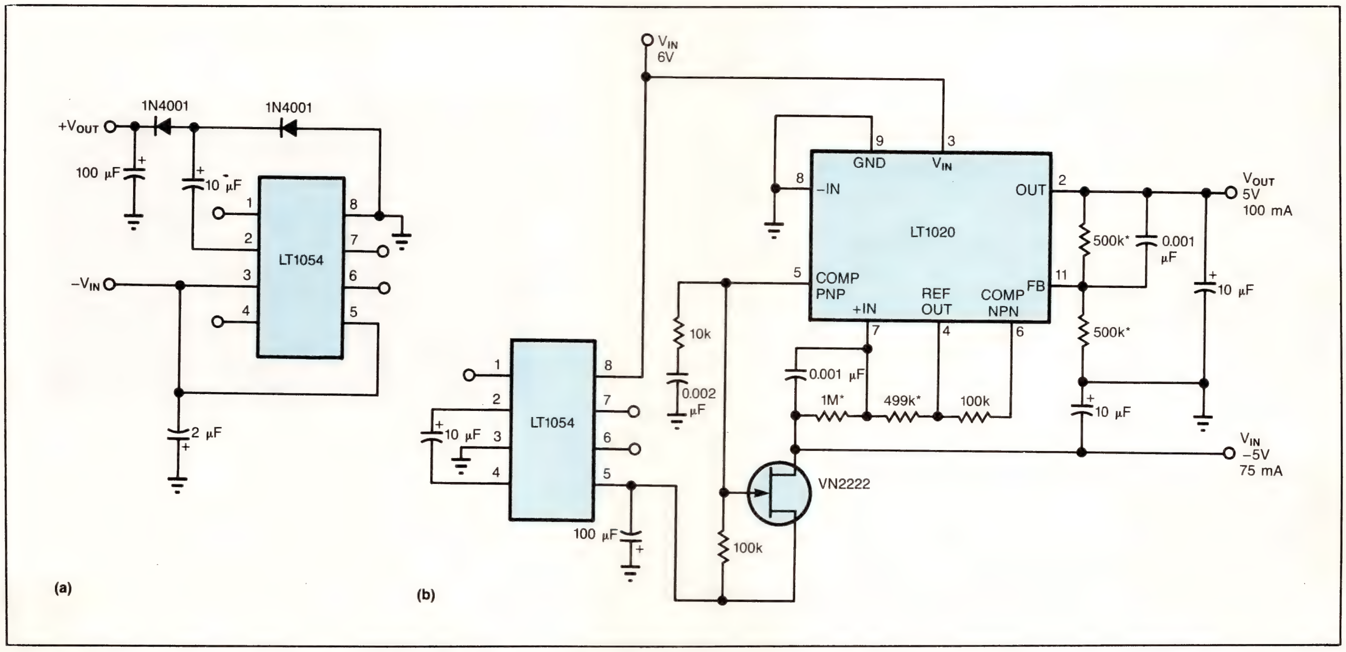


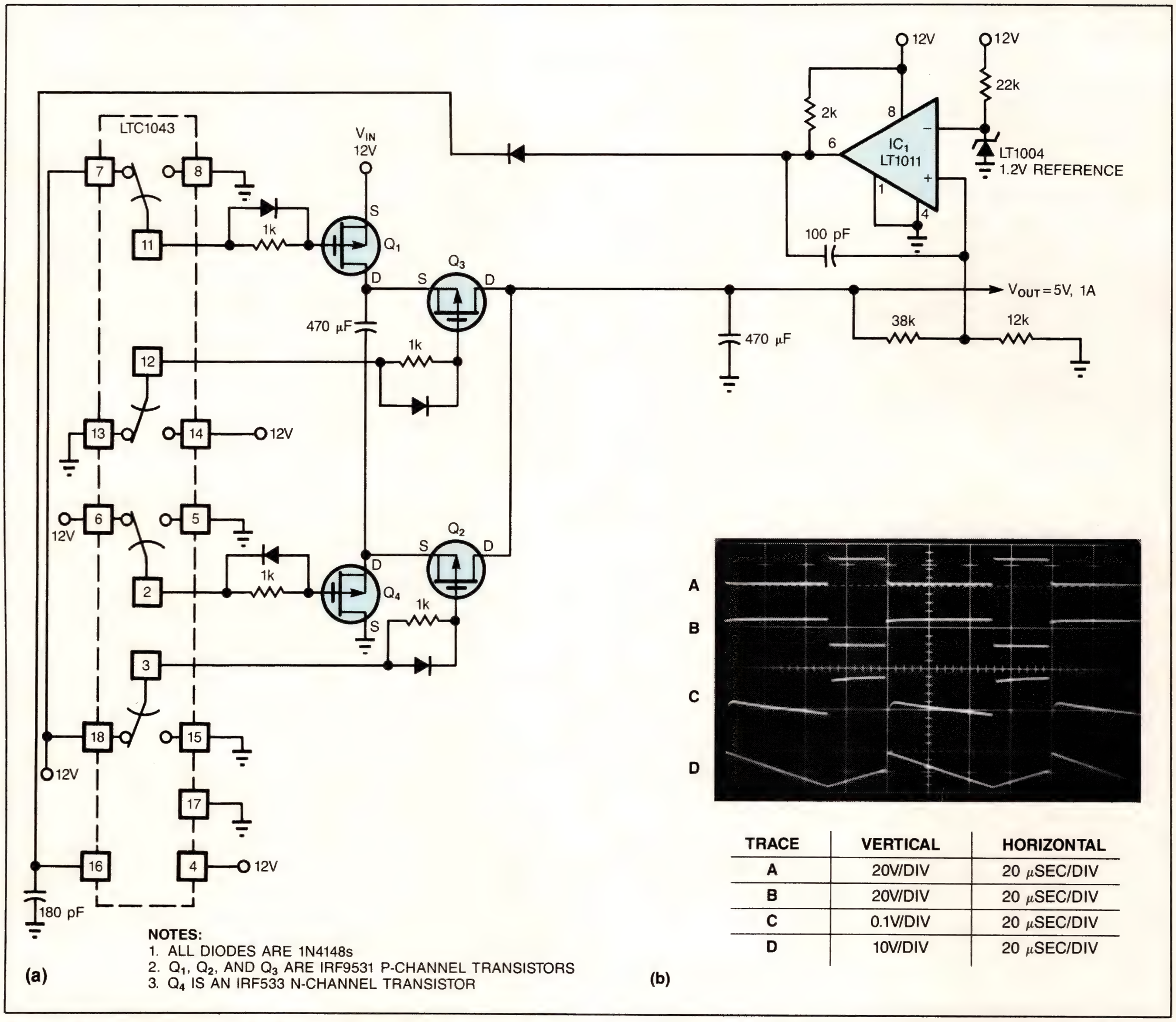
***Fig 3—By adding some steering diodes to Fig 2's circuit,** you can convert a negative input into a positive output **(a)**. By modifying the circuit somewhat **(b)**, you can develop a converter that transforms a 6V input into ±5V outputs.*

Capacitors can store energy; thus, they can serve as the basic transfer element in dc/dc-conversion processes.

flows through both capacitors and charges them to furnish load current. During the parallel phase, both capacitors work to provide half the load current. **Fig 4b** illustrates the LTC1043-supplied drive inputs to Q_3 and Q_4 (traces A and B, respectively). Q_1 and Q_2 receive similar drive inputs from pins 11 and 3 of the LTC0143. The diode-resistor networks ensure that the series-parallel phase switches see no simultaneous drive pulses.

If the circuit didn't include IC_1, its output would equal $V_{IN}/2$, but IC_1 and its associated components reduce the converter's output to 5V. When the circuit is in the series phase, the output has a rapid transition in the positive direction (trace C). When the output exceeds 5V, IC_1 trips and forces the LTC1043's oscillator pin high (trace D). This transition truncates the LTC1043's triangle-wave oscillator cycle.

The truncation forces the circuit into the parallel phase, and the output slowly diminishes until the beginning of the LTC1043's next clock cycle. IC_1's output diode ensures that any sharp transitions from the 180-pF capacitor will have no effect on the triangular down-



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	20 µSEC/DIV
B	20V/DIV	20 µSEC/DIV
C	0.1V/DIV	20 µSEC/DIV
D	10V/DIV	20 µSEC/DIV

***Fig 4—You can develop a high-power converter** by adding some discrete devices to the basic switched-capacitor circuitry **(a)**. The diode-resistor networks ensure that the series-parallel phase switches (Q_1 and Q_2) see no simultaneous drive pulses **(b)**.*

slope waveform. The feedback loop regulates the output by controlling the turn-off point of the series phase. The circuit's power MOSFETs easily handle any high transient currents, and the circuit's efficiency measures 83%. EDN

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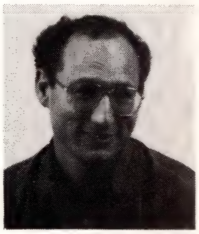
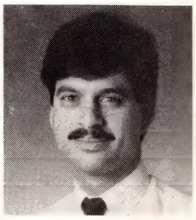
Authors' biographies



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



Brian Huffman is an applications engineer at Linear Technology Corp. A member of the IEEE, he holds a BSET degree from Indiana State University and an MSEE from Santa Clara University. In his spare time, Brian enjoys plays, concerts, and the beach, and he likes to travel.

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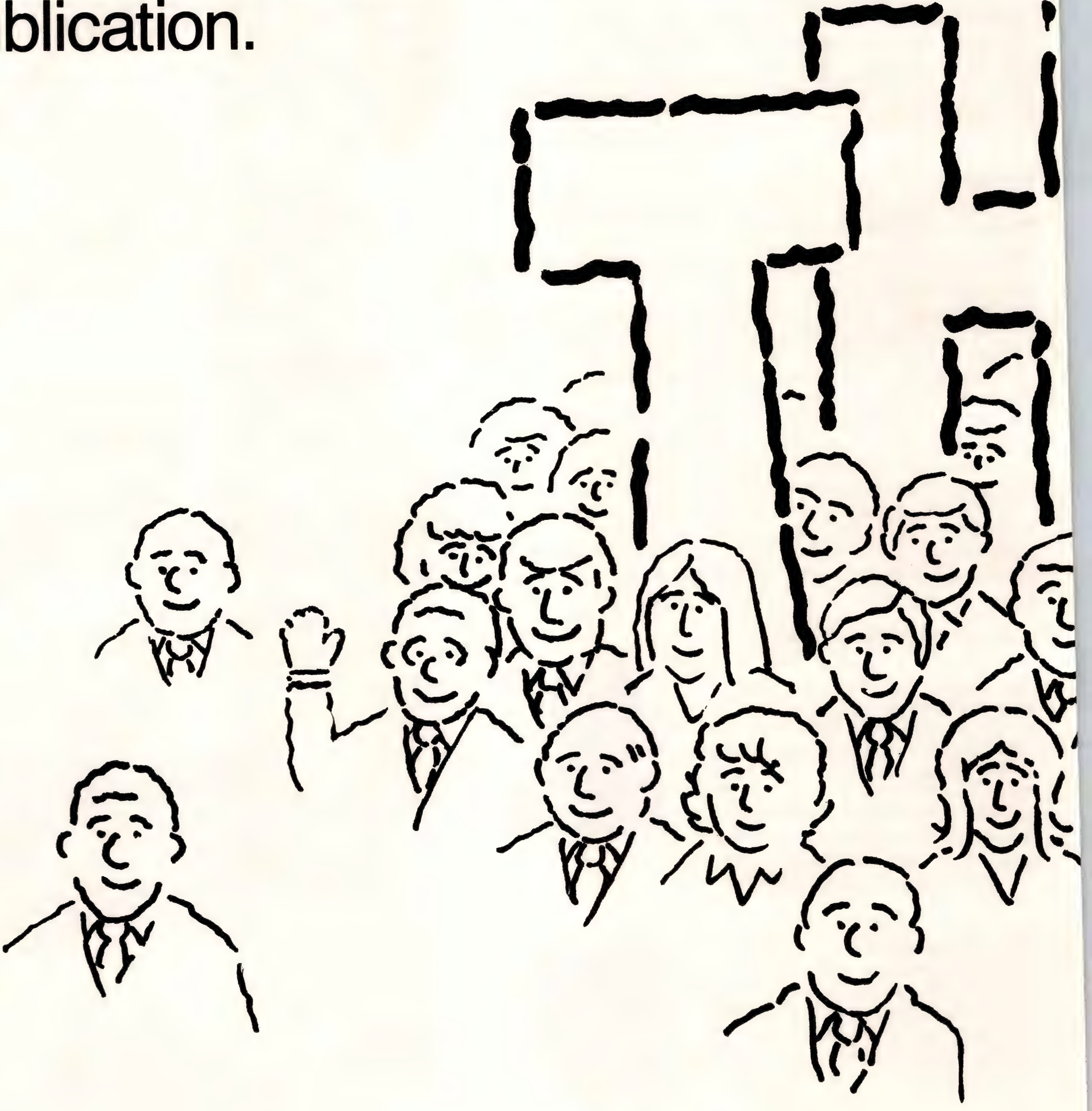

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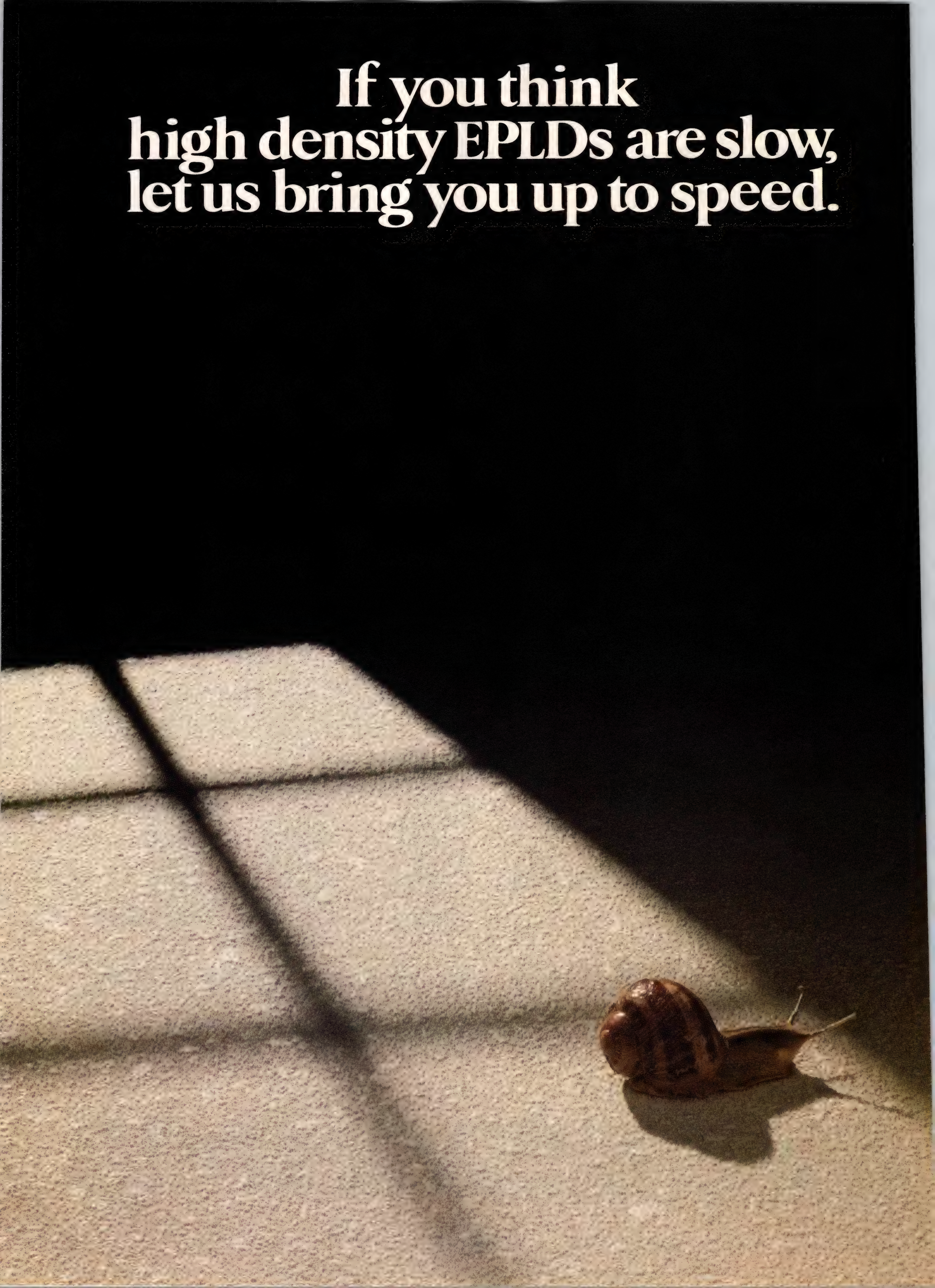
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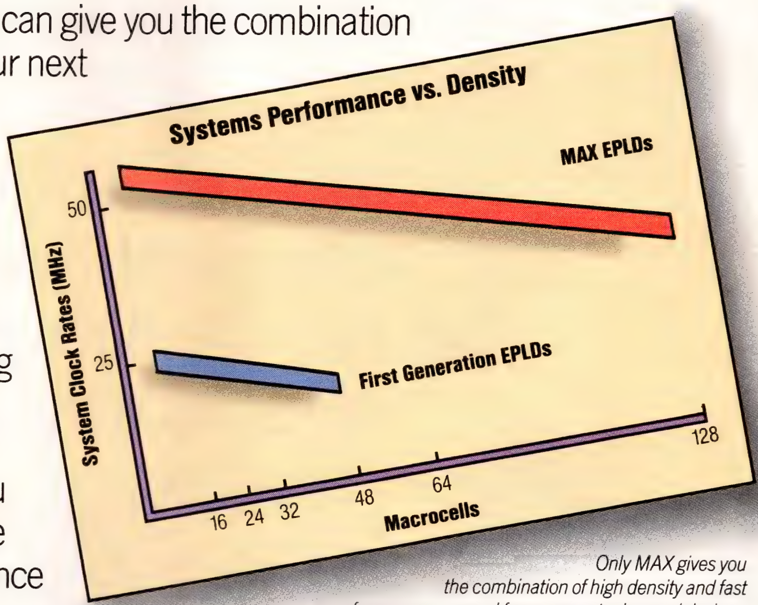

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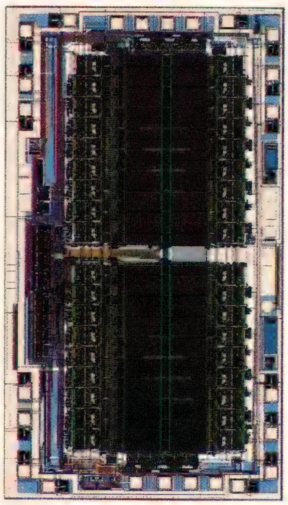

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Card-edge emulation facilitates debugging in design and test

Although in-circuit emulators (ICEs) can be invaluable in debugging μP-based systems in the development lab, attempting to use ICEs as production-test tools can often cause problems. To avert these problems, you can change the way you connect the emulator to the board under test.

Art Lizotte, *Complementronics Inc*

Minimizing development time and ensuring testability are two important factors in the development and manufacture of printed-circuit boards that contain embedded microprocessors. In-circuit emulators can help to control these factors, but one often-troublesome requirement for using an emulator is the need to remove the μP from the board to plug in the emulator probe. You can't always remove chips—factors such as pc-board area, mechanical characteristics, and packaging considerations (for example, the use of surface-mount technology) can necessitate soldering them in. And, though you might use sockets on prototype boards, on production boards there's a good possibility that you won't be able to afford the luxury. One solution to the problem is card-edge emulation.

Card-edge emulation is a way to perform all aspects of emulation without unsoldering the μP from the pc board. To use card-edge emulation, you must be able to electrically disable the μP on the board under test (BUT) while you have the emulator connected to the board. You disable the μP by using either the bus-arbitration lines or the reset line to place the system microprocessor buses in the high-impedance state. You can use many off-the-shelf in-circuit emulators by replacing the probe with your own assembly, consisting of a cable, a card, and a connector that mates with the BUT. Ideally, your custom probe mates with the connector that connects the board to the system in which it normally operates. Sometimes, however, pc-board-space or pin-count limitations can require you to design the BUT with an extra connector to be used only for emulation. Even when you have to design in a dedicated connector, though, card-edge emulation can pay for itself.

Emulators can help in production test

Well-written diagnostic routines are crucial in locating faulty components, but when designers need to add new features to a system whose ROM space is nearly full, those diagnostics are usually the first items to be sacrificed. Reduced diagnostic capability makes it much harder to identify a defective part, so if you're considering making firmware changes, don't overlook the higher testing costs they'll incur.

Logic analyzers, which are often used for troubleshooting in production, can only trace the execution of programs that reside in the system. There-

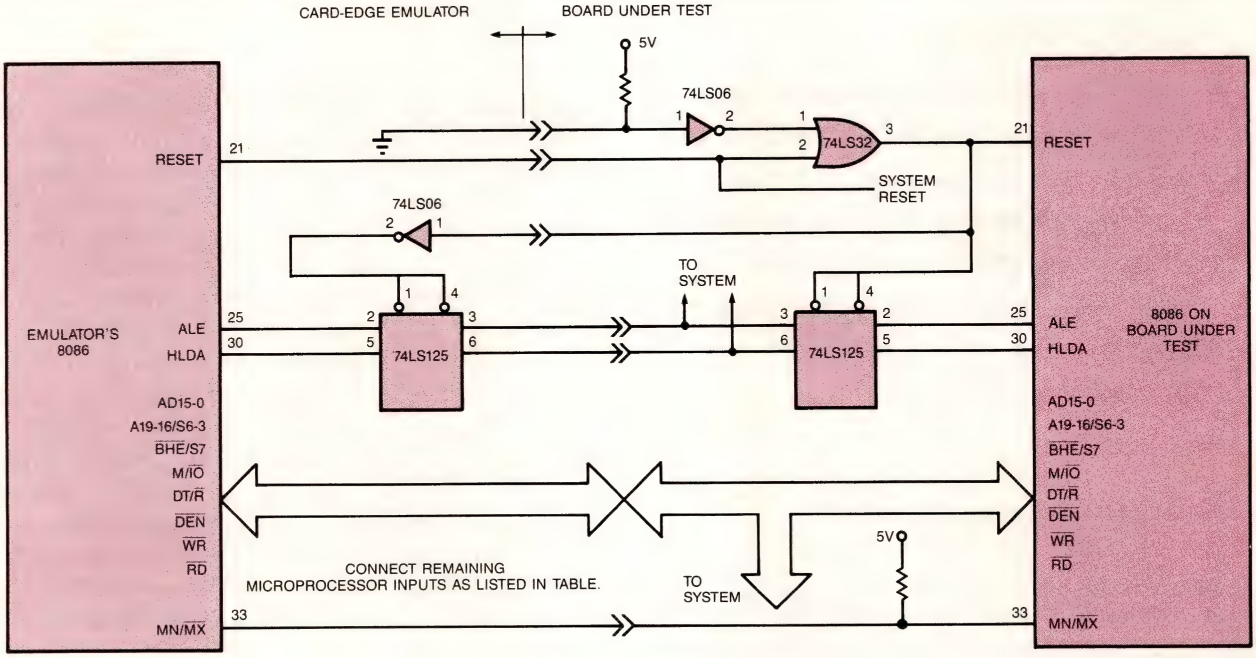
Although you might use sockets on prototype boards, for production boards you probably won't be able to afford the luxury.

fore, if you curtail the diagnostic routines, a logic analyzer may not let you see a problem's potential source. Emulators, however, have memory of their own, so they can execute extended diagnostic routines that are too long to fit into your system's ROM. Emulators also let you control program execution to avoid the possibility of damage caused by runaway code.

You can use an emulator to perform a board-level functional test. The ability to trace and control the execution of code, and to display and modify the contents of target-system memory locations and registers, is a standard feature of most emulators. This capability can let you simulate real-world conditions. By placing execution-control and trace commands in a "script" (a file—usually text—that simulates operator input), you can automate a test process for use in production.

To solve a problem systematically, you should identify its possible causes, eliminating the ones that don't apply. This process of elimination is a major part of debugging—not only in production test but in product design and development. Because it can help shorten the list of a problem's possible causes, card-edge emulation can be an important tool for development engineers. During development, for example, you can often trace intermittent malfunctions to a µP socket whose contacts are suffering from metal fatigue because the socket has been plugged and unplugged too many times.

If you're using an in-circuit emulator to diagnose an intermittent system malfunction, and the ROM-



CARD-EDGE CONNECTIONS FOR REMAINING 8086 MINIMUM-MODE INPUTS

INPUT	EMULATOR PIN	BOARD-EDGE PIN
READY	22	22
INTR	18	18
$\overline{\text{TEST}}$	23	23
NMI	17	17
CLK	19	19
HOLD	31	31

Fig 1—For an 8086 in minimum mode, *you can implement card-edge emulation by placing only three ICs on the assembly that replaces the in-circuit emulator's probe.*

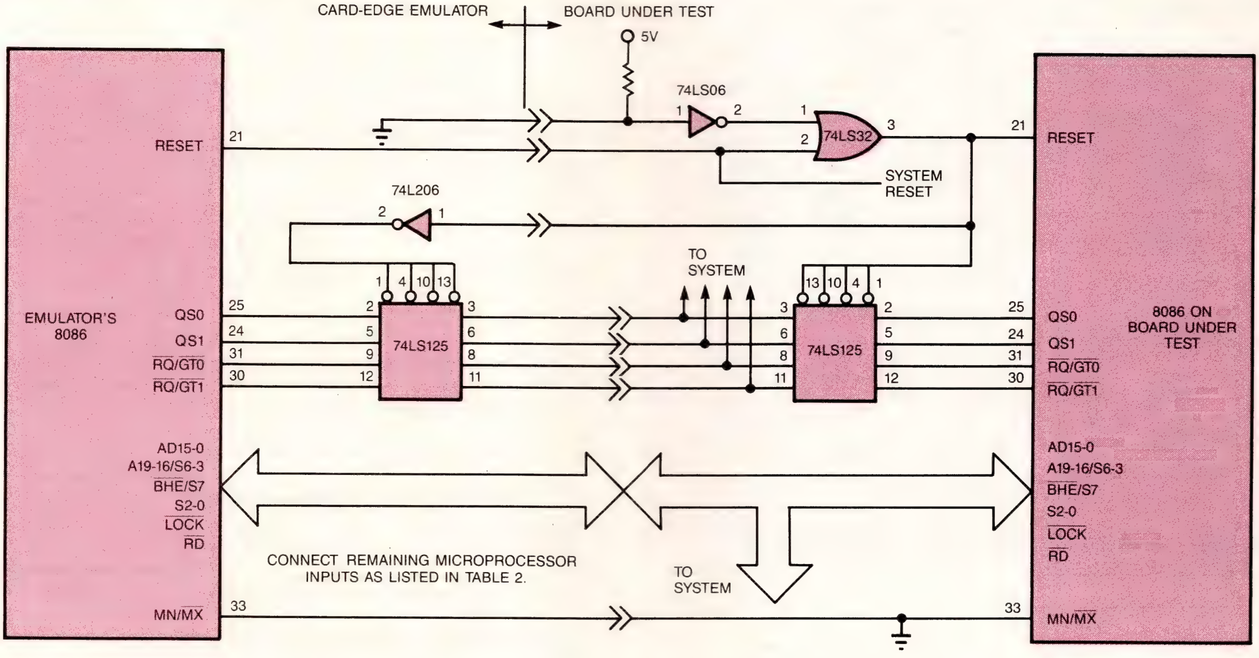
resident diagnostics pass but the emulation-memory-resident diagnostics fail, you can spend hours trying to determine where the problem lies. The possible culprits are the ROM-resident diagnostic code, the ROM-resident operating code, the RAM-resident diagnostic code, the system hardware, and the connection between the emulator and the BUT. The classic reason for the problem, of course, is a system-hardware malfunction that's outside the scope of the ROM-based diagnostic routines but within the scope of the more comprehensive emulator-based diagnostics. Often, however, the problem is merely an open address line on the μP socket.

When you use card-edge emulation, the processor is always in the system. If a malfunction occurs, you first run the diagnostic routines embodied in the system firmware. If the firmware-resident tests pass, you can connect the emulator and run the diagnostic routines that reside in emulation memory. If the tests still fail, the list of possible culprits is the same, but a connection problem between the μP and the system is far less likely.

Whether you're working in production or in design, card-edge emulation can satisfy your needs for developing and testing a system based on an embedded μP. Two system designs demonstrate the technique.

Three ICs permit 8086 card-edge emulation

Your first step in implementing card-edge emulation is to determine how to disable the μP. Once you've



CARD-EDGE CONNECTIONS FOR REMAINING 8086 MAXIMUM-MODE INPUTS

INPUT	EMULATOR PIN	BOARD-UNDER-TEST PIN
READY	22	22
INTR	18	18
$\overline{\text{TEST}}$	23	23
NMI	17	17
CLK	19	19

Fig 2—For an 8086 in maximum mode, *implementing card-edge emulation is only slightly more complicated than it is for an 8086 in minimum mode* ***(Fig 1).***

Firmware changes may reduce a board's diagnostic capabilities, so when you consider making such changes, remember that testing may cost more.

determined that, note which signals do not enter the high-impedance state; you'll have to provide 3-state buffers for these signals. For example, you can disable Intel's 8086 by asserting its Reset line. The state of the MN/$\overline{\text{MX}}$ line determines which signals will require 3-state buffers. If your system doesn't use these lines, you obviously don't need to buffer them.

Table 1 shows these signals; **Figs 1** and **2** show the schematics for the minimum and maximum modes, respectively. After you assert Reset, the 8086 will wait until the end of the next clock-low period to place certain signal lines in a high-impedance state **(Fig 3)**. Because the clock's half-period duration is so short, the delay generally won't cause a problem. However, if necessary, you can take care of the delay by adding a flip-flop on the emulator side of the card edge; this action will delay the enable signal by one clock cycle. Thus, by adding a maximum of six devices—three on the µP-based board and three more on the probe—you can implement card-edge emulation. (If some of the ICs on the BUT contain unused gates, you may not have to add as many devices to the BUT.)

In implementing card-edge emulation, you should be mindful of several design considerations. The first is that an emulator acts as much like the real microprocessor as possible. Most emulators sample control signals by using flip-flops for internal synchronization and control. This technique can cause problems if the signals have glitches or ringing on their edges. For instance, you must assert the Reset line of the 8086 for at least four clock cycles before the CPU will recognize it. If a glitch causes the emulator to latch the Reset

TABLE 1—8086 BUS DURING RESET

SIGNALS	CONDITION
AD15-0	3-STATE
A19-16/S6-3	3-STATE
$\overline{\text{BHE}}$/S7	3-STATE
$\overline{\text{S2}}$/(M/$\overline{\text{IO}}$)	DRIVEN TO "1," THEN 3-STATE
$\overline{\text{S1}}$/(DT/$\overline{\text{R}}$)	DRIVEN TO "1," THEN 3-STATE
$\overline{\text{S0}}$/($\overline{\text{DEN}}$)	DRIVEN TO "1," THEN 3-STATE
LOCK/($\overline{\text{WR}}$)	DRIVEN TO "1," THEN 3-STATE
$\overline{\text{RD}}$	DRIVEN TO "1," THEN 3-STATE
($\overline{\text{INTA}}$)	DRIVEN TO "1," THEN 3-STATE
(ALE)	0
(HLDA)	0
$\overline{\text{RQ}}$/$\overline{\text{GT0}}$	1
$\overline{\text{RQ}}$/$\overline{\text{GT1}}$	1
QS0	0
QS1	0

NOTE:
SIGNALS IN PARENTHESES ARE MINIMUM-MODE SIGNALS.

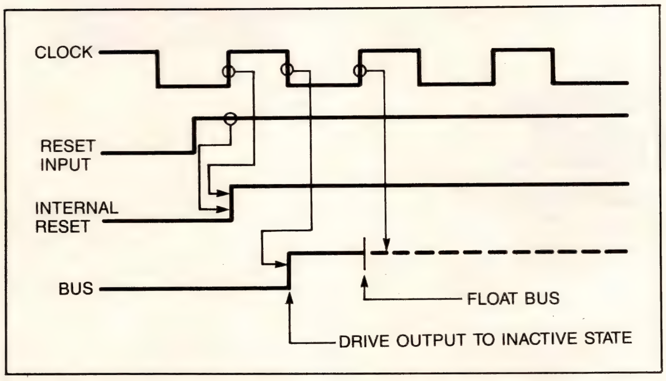


Fig 3—When the 8086's Reset input goes high, *the chip waits until the next rising clock edge to set the internal reset high, and it waits until the second rising clock edge to float the bus.*

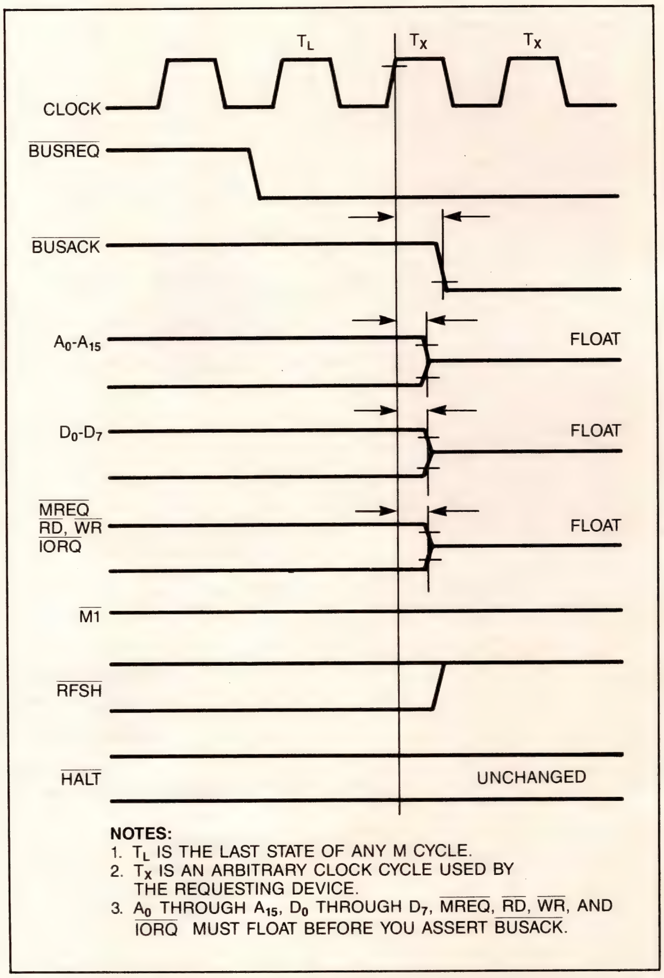


Fig 4—After a bus request, the Z80 *floats the address and data buses before the second falling clock edge appears.*

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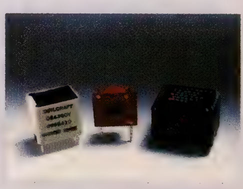

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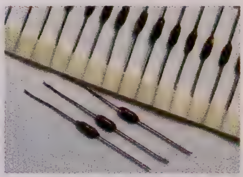

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If you haven't provided the necessary hooks at the design stage, you'll have to rely on means other than emulation to test your board.

signal for fewer than four clock periods, it can arbitrarily reset internal hardware within the emulator but fail to reset the 8086. This condition will almost certainly disrupt program execution. To prevent glitches from causing spurious resets, you can add series resistors to the Reset line on the emulator board that you design to mate with the card edge. Ringing on the clock line can also cause problems that necessitate terminating the line. (**Ref 1** spells out termination options.)

Card-edge emulation of the Z80 is simple

You can disable the Zilog Z80 by asserting the BUSREQ line through the card-edge connection. **Fig 4** shows that the Z80 floats its buses at the rising edge of the next clock cycle and then asserts BUSACK. You should buffer the address and control lines on the emulator side of the card edge to avoid contention between the emulator and onboard-processor address buses. The data bus does not need buffering, because emulators usually configure the data bus as a group of inputs during an internal reset (**Fig 5**). The onboard processor will have relinquished the address bus to the emulator long before you release the emulator's Reset line. To implement card-edge emulation for the Z80, you need to add, at most, three devices to the BUT and two to the emulator probe. These simple devices allow you to use an emulator to perform extensive tests on a Z80-based board.

You can pull back from the edge

How you connect the emulator to the BUT will depend on your production and system requirements. Assigning pins on an existing board-edge connector is the least expensive connection technique. If pin limitations preclude that approach, but there's room on the board, you can place a dedicated test connector near the card's edge. You can use almost any convenient location for such a connector, but keep in mind the lengths of copper and the area in which the signals will pass. Obviously, running all the address lines through a noise source such as a switching power supply could cause problems later. If existing board-edge connectors can't accommodate all the signals you need for the emulator interface, and there's no room for an additional connector, you can even use a bed-of-nails fixture. The possibilities for connecting to the BUT are numerous, but if you haven't provided the necessary hooks at the design stage, you'll have to rely on means other than emulation to test your board.

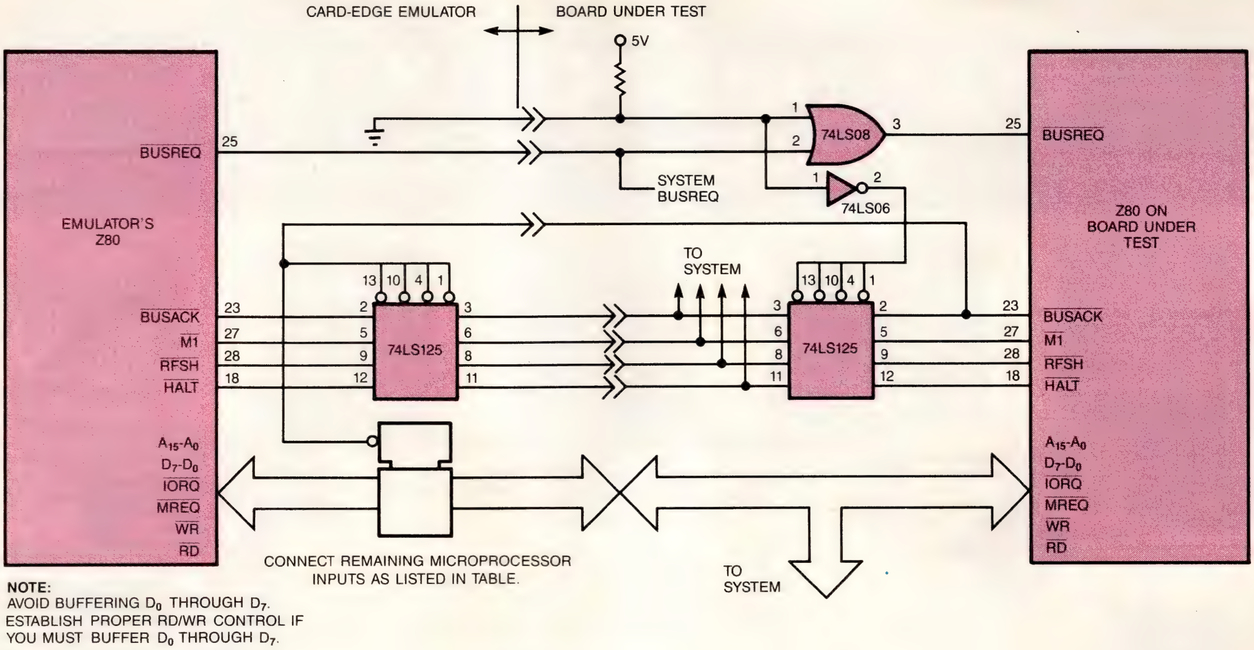
For the two μPs discussed here, the connector will require at least 41 points. They comprise all of the microprocessor's signals, including 5V as well as the

Emulators prove useful in production

For years, development engineers have used in-circuit emulators in developing systems with embedded microprocessors. Production-test departments, however, have not used ICEs extensively because of the requirement for removing the microprocessor. Card-edge emulation provides production test with the hooks needed for testing complex systems.

Emulators offer many useful functions to test engineers. Displaying and modifying internal memory locations of ICs are only two of the capabilities of emulators. An emulator also lets you start and stop programs to control the progress of a test. Standalone logic analyzers, on the other hand, can only monitor what the system has done. They can't interrogate the processor's registers or a UART's status register. By loading programs into an emulator's memory, you can perform extensive diagnostic functions, yet avoid encumbering the system firmware with voluminous or frequently modified code. Operations such as calibration and EEPROM initialization can also be performed through an emulator interface rather than by executing code resident in the system.

Now that the personal computer is making its way onto the production floor, many people have suggested that emulators should be based on PCs. A large number of vendors offer PC-based emulators. With their integral disk drives, PC-based emulators can save emulation data for later analysis in production test. For example, data stored during the testing of a known-good unit could help you diagnose a problem that afflicts an entire production run (say, when each member of the run is built with a single defective part from a faulty lot). Only your imagination limits the possible uses of emulators in testing.



CARD-EDGE CONNECTIONS FOR REMAINING Z80 INPUTS

INPUT	EMULATOR PIN	BOARD-UNDER-TEST PIN
$\overline{WAIT}$	24	24
$\overline{INT}$	16	16
$\overline{NMI}$	17	17
$\overline{RESET}$	26	26

***Fig 5—Card-edge emulation for the Z80,** as for the 8086, requires very little hardware that's external to the emulator.*

signal that, in the low state, disables the system microprocessor. The 5V supply powers not only your board but also any components on the probe—emulators determine when you have the components connected in circuit by sensing the load on the 5V line. If there are pins to spare, you should use as many of them as possible for ground connections. A solid ground will provide a better reference for the emulator and will improve the signal quality. You need to place the extra grounds so that they'll act as shields around pins carrying signals that produce (or are susceptible to) glitches.

Microprocessors have traditionally presented a testing challenge. Card-edge emulation can be an especially convenient solution to problems with testing µP-based boards, because it lets designers and test engineers use the same equipment. Overall:

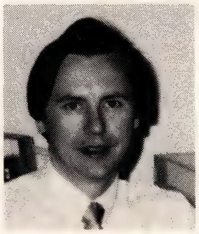
- Development is faster. Designers don't waste time solving problems unrelated to design.
- Testing is easier. A very small amount of test-support hardware is on the BUT, and the emulator provides the necessary control.

Card-edge emulation not only satisfies testing needs during the development of an embedded microprocessor system, but also fulfills long-term testing requirements during production. EDN

Reference

1. Pace, Charles, "Terminate bus lines to avoid overshoot and ringing," *EDN*, September 17, 1987, pg 227.

Author's biography



Art Lizotte operates Complementronics, a firm that consults on the development of systems based on embedded microprocessors. He started Complementronics a year ago; before that he worked as a systems engineer at Hewlett-Packard. Art holds a BSEE and an MS in computer science from Stevens Institute of Technology (Hoboken, NJ), and he's a registered professional engineer. He collects coins and stamps, and enjoys skiing and hiking.

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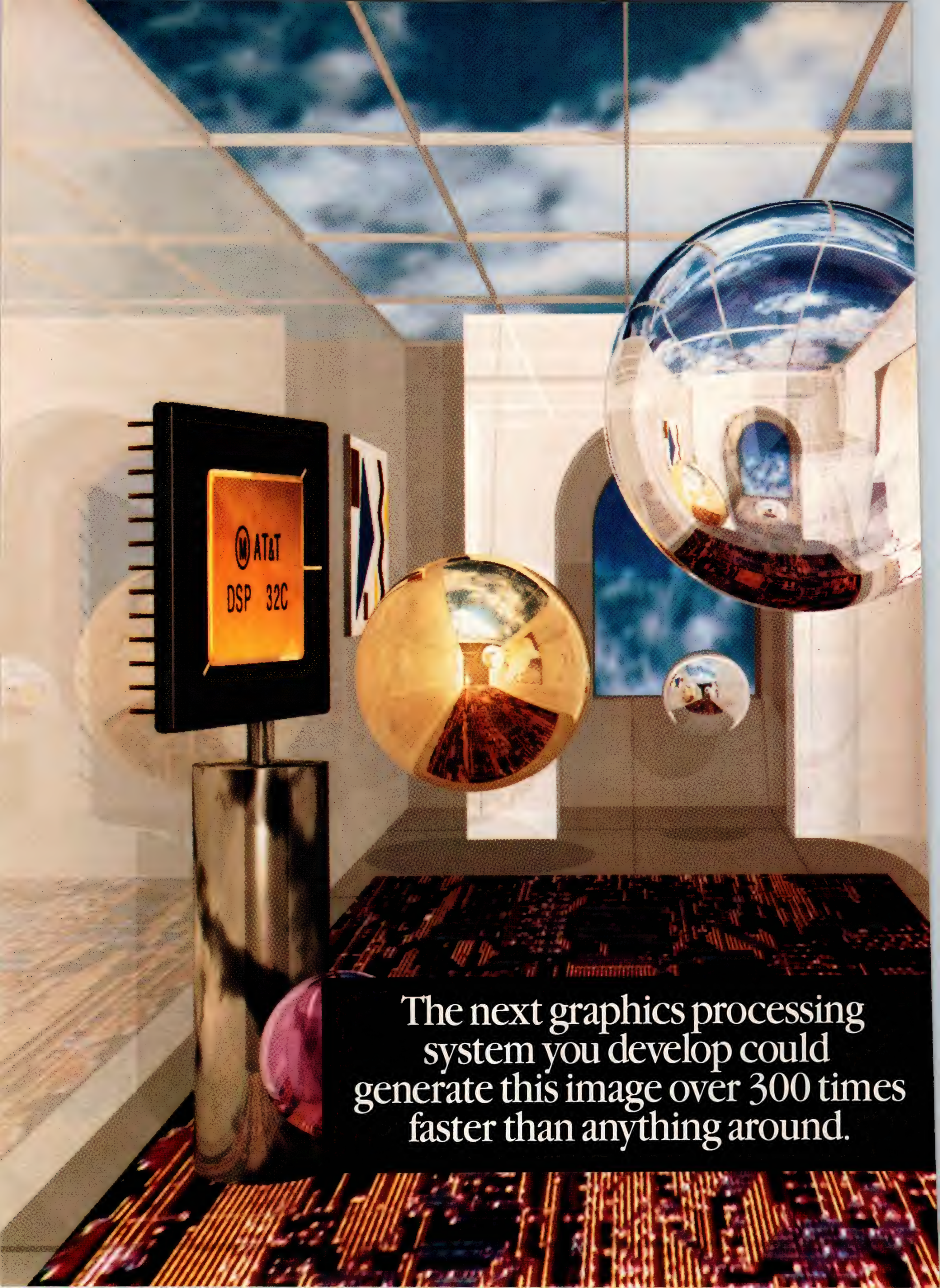
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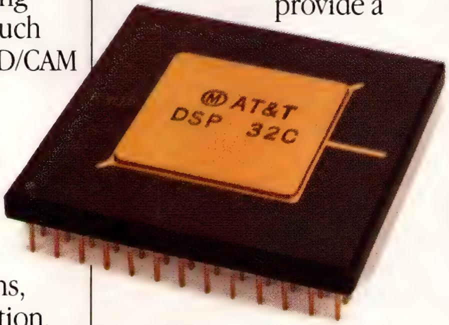

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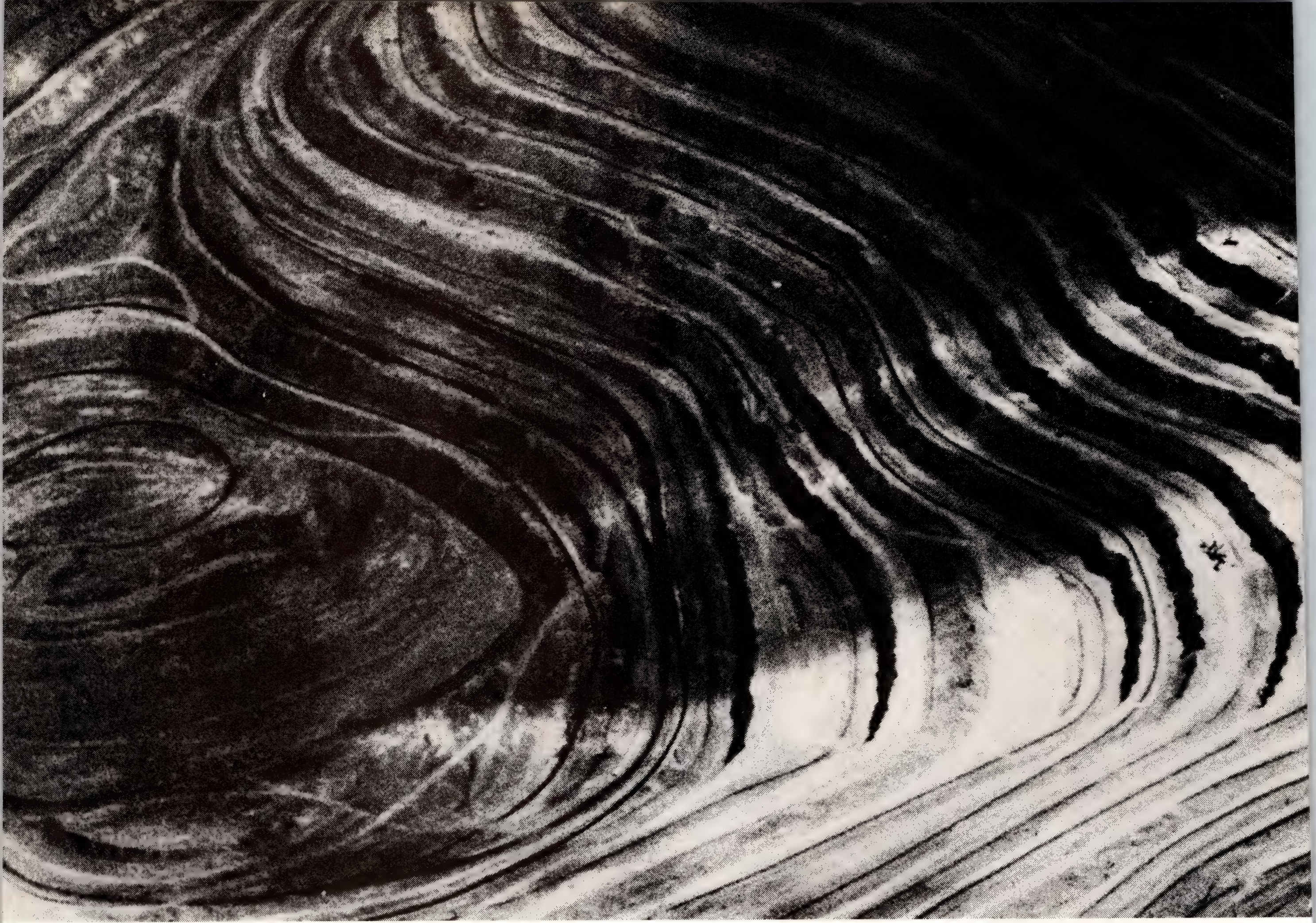

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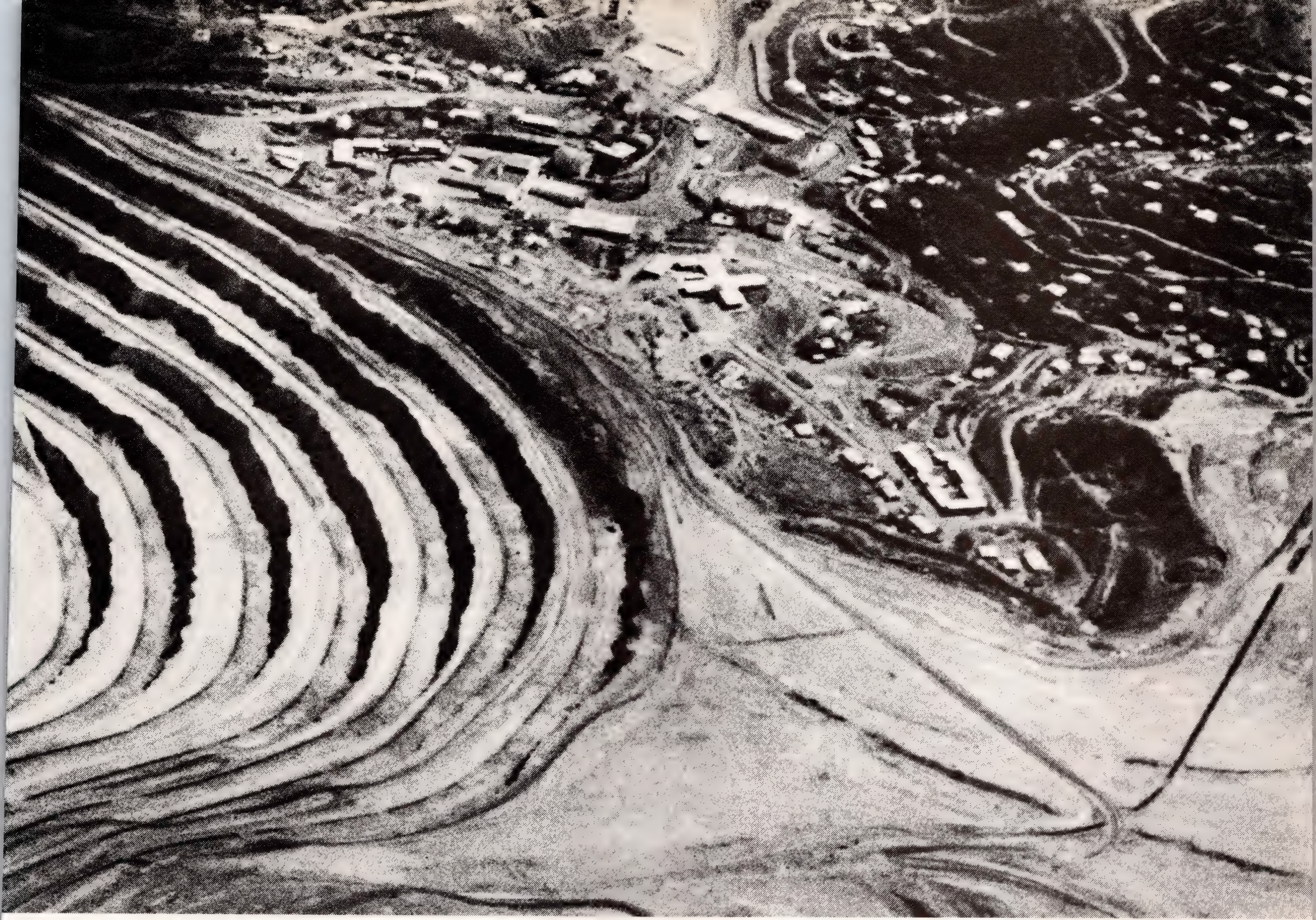

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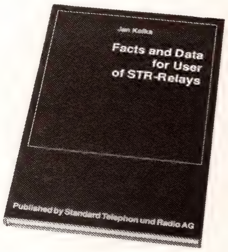

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Choosing a network for local industrial control

The system designer has a bewildering number of choices for networks in local industrial-control applications. Since many of these networks interface with STD Bus products, the designer should consider how easily a network can be implemented with these offerings.

Rob Davidson, Robert Metz, and Alan Beverly,
Ziatech Corp

Local industrial-control networks often must interconnect a variety of computers to STD Bus boards. The boards are attractive in this setting because they can withstand the harsh environment of the factory floor and can function as remotely controlled embedded nodes in real-time applications. As the system designer, you are faced with the choice of how to link these elements together. For example, you could connect the nodes through serial ports and write your own communication software or you could use a standard local-area network (LAN) and a commercially available network software package.

On the factory floor, a local industrial network is usually a subset of a larger backbone network that links a company's administrative, marketing, and manufacturing processes together **(Fig 1)**. The local industrial network independently performs process-control tasks and interfaces with the backbone network through a gateway. The cost/performance tradeoffs for selecting a local industrial network include topology flexibility, cabling requirements, data throughput, reliability, and ease of maintenance. Economy and reliability steer a

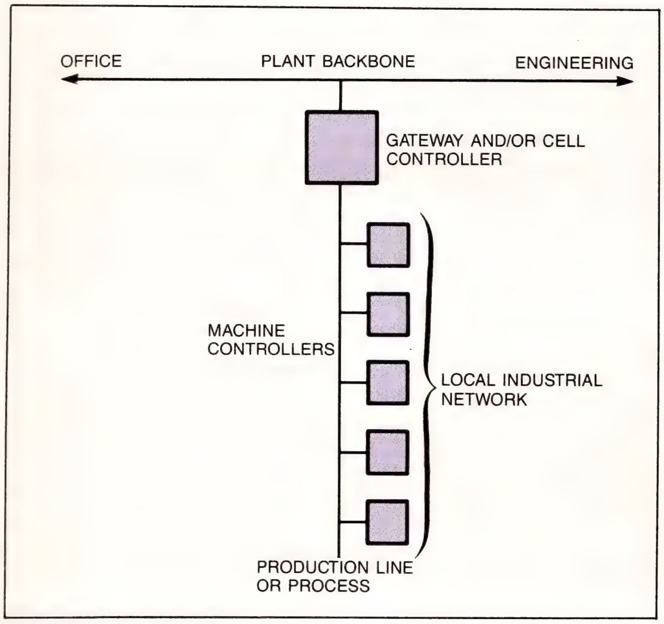

Fig 1—Typical local industrial networks connect to a large plant backbone *through gateways or cell controllers.*

TABLE 1—COMPARISON OF EIA STANDARDS

PARAMETER	RS-232C	RS-423	RS-422	RS-485
MODE OF OPERATION	SINGLE ENDED	SINGLE ENDED	DIFFERENTIAL	DIFFERENTIAL
NUMBER OF DRIVERS AND RECEIVERS ALLOWED ON LINE	1 DRIVER 1 RECEIVER	1 DRIVER 10 RECEIVERS	1 DRIVER 10 RECEIVERS	32 DRIVERS 32 RECEIVERS
MAXIMUM CABLE LENGTH (FT)	50	4000	4000	4000
MAXIMUM DATA RATE (BITS/SEC)	20k	100k	10M	10M
MAXIMUM COMMON MODE VOLTAGE	±25V	±6V	+6V −0.25V	+12V −7V
DRIVER OUTPUT SIGNAL	±5V MIN ±15V MAX	±3.6V MIN ±6.0V MAX	±2V MIN	±1.5V MIN
DRIVER LOAD	3 kΩ-7Ω	450Ω MIN	100Ω	60Ω
DRIVER SLEW RATE	30V/μSEC MAX	• CONTROLLED • DETERMINED BY CABLE LENGTH & DATA RATE	NA	NA
DRIVE OUTPUT RESISTANCE (HIGH Z STATE) — POWER ON	NA	NA	NA	±100 μA MAX $-7V \le V_{CM} \le 12V$
DRIVE OUTPUT RESISTANCE (HIGH Z STATE) — POWER OFF	300Ω	±100 μA MAX AT ±6V	±100 μA MAX $-0.25V \le V_{CM} \le 6V$	±100 μA MAX $-7V \le V_{CM} \le 12V$
RECEIVER INPUT RESISTANCE	3 kΩ-7 kΩ	>4 kΩ	>4 kΩ	>12 kΩ
RECEIVER SENSITIVITY	±3V	±200 mV	±200 mV $-7V \le V_{CM} \le 7V$	±300 mV $-12V \le V_{CM} \le 12V$

designer toward the serial-port standards set by the Electrical Industries Association (EIA), those set by the Bitbus, and those set by Arcnet.

Although they aren't usually regarded as network standards, the EIA serial-port standards define low-cost methods for connecting computers together. The EIA refers to these standards as RS-232C, RS-422, RS-423, and RS-485. Most STD Bus computers feature at least one of these types of serial ports, thus a serial connection is an inexpensive and convenient way to implement a simple industrial network.

The RS-232C standard specifies that data be transmitted single-endedly over short distances (50 ft or less) and at slow data rates (300 to 19.2k baud). The RS-423 standard extends the single-ended transmission rate to 100k baud for distances as long as 300 ft and extends the maximum distance to 4000 ft for data rates as high as 1k baud. The RS-423 also has a wave-shaping specification to control reflections and emissions and calls for high-impedance drivers that don't load the transmission line when they are powered off.

The RS-422 specification defines differential data transmission at rates as high as 10M baud for a distance of 40 ft and 100k baud for a distance of 4000 ft. This standard lets you build a multipoint network with one driver and 32 receivers on the link. You can realize a multipoint network with multiple drivers and receivers using the RS-485 standard. This specification has the same transmission rate and distance specification as the RS-422 but permits 32 drivers and 32 receivers on the same link.

The EIA standards specify the electrical characteristics of drivers and receivers; a summary of these characteristics is shown in **Table 1.** Note that the standards do not recommend a protocol. A communication protocol must be defined by the system designer.

There are a variety of communication controller ICs that implement synchronous or asynchronous protocols. These ICs connect directly to the drivers and receivers to realize serial networks using the EIA standards. A communication chip, such as National Semiconductor's 8250 UART, executes low-level protocols for transmitting and receiving asynchronous bytes of data **(Fig 2a).**

RS-232C and RS-423 are low-cost standards for connecting two computing units together; RS-422 and RS-485 are suitable for low-cost multipoint networks. A multipoint network, however, requires protocol functions above the lower-layer protocols for error detection and network routing. The host processor must provide this information in software. An example pseudocode listing for these protocol functions is shown in **Listing 1.** You can implement these functions by writing your own proprietary routines or by using one of the commercially available communication libraries that run on PC-compatible STD Bus systems.

A standard package offers compatibility

Since serial networks constructed in this manner are nonstandard and generally low speed, you might want to consider a standard package developed for the RS-485 specification. The Bitbus is an I/O network that was developed by Intel Corp in 1983 to overcome the problems associated with nonstandard factory-floor communication links. It is a serial control bus that uses the RS-485 standard for the physical level and the synchronous data link control (SDLC) protocol for the data-link level. The Bitbus's master controller can

LISTING 1

RS-422/485

Initialize the single-network master and the slave machines by assigning a unique ID to each unit.

A host processor must generate the data packets. First, it transmits a header containing a Destination ID, Source ID, Command Code, Sequence Number, and Data Length. It then places the data after the header and follows it with an error-checking trailer.

Every machine on the network monitors the Destination ID for each transmission to see if a packet is intended for that machine.

The master issues an Invitation to Transmit (IT) command to each slave based on a priority scheme.

Each packet transmission invokes an Acknowledgment (ACK) or Negative Acknowledgment (NAK) from the recipient.

The master is the only machine that can initiate a transmission other than an ACK or NAK.

A slave that dosen't receive a NAK or ACK signal after it transmits a data packet retransmits the packet the next time it receives an IT command from the master. The Sequence Number eliminates any duplicate packets.

communicate with as many as 250 slave distributed control modules (DCMs).

Manufacturers have developed a variety of DCMs with preconfigured software ranging from A/D converters to video control modules. Each module may support as many as 16 asynchronous tasks for monitoring and control. Data is transferred over the Bitbus in one of two modes: the synchronous mode or the self-clocked mode. The synchronous mode provides high performance over short distances. This mode permits 28 nodes to operate on a 30m bus at transmission speeds between 500k and 2.4M baud. The synchronous mode uses two differential signal pairs: one for data and one for the data clock. The data clock always originates from the transmitting node.

The self-clocked mode lets you operate over longer distances at two possible bit rates: 375k and 62.5k baud. In this mode, a data rate of 375k baud is possible for distances as long as 300m and a rate of 62.5k baud is possible for link lengths as long as 1200m. You can connect as many as 28 nodes per segment, and you can interconnect segments via repeaters to handle as many as 250 nodes. The self-clocked mode uses two differential signal pairs: one for data and one for the request-to-send (RTS) control line. The data signal utilizes non-return-to-zero inverted (NRZI) encoded data. In this encoding scheme, the data and the clock are combined onto the same signal pair.

The SDLC protocol for the Bitbus predefines the addresses for the nodes on the bus; therefore, the programmer only has to format the data packets for transmission and determine whether the received data is valid. Typically, communication between a node and the Bitbus controller is through an additional I/O card located on the node's STD Bus. This card handles the low-level protocols and requires customized software for each application.

If a local industrial network requires more features than the Bitbus offers, you need to consider a LAN. Arcnet, for example, is a LAN developed by Datapoint Corp in 1976 and is widely used in factory environments. Although it is a proprietary protocol, Arcnet is a de facto standard in an estimated 1,000,000 currently installed nodes. **Table 2** compares some of the features of Arcnet with the EIA standards and the Bitbus. You implement the protocol using the COM 9026 chip set, which is made under license by Standard Micro Systems (Hauppauge, NY) and NCR (Miamis-

TABLE 2—NETWORK FEATURE COMPARISON

NETWORK NAME	ARCNET	RS-422/485	BITBUS
PRIMARY TOPOLOGY	MULTIDROP, STAR	MULTIDROP	MULTIDROP
DISTANCE WITHOUT REPEATERS	1000 FT MULTIDROP 2000 FT STAR	4000 FT	100-4000 FT
NUMBER OF NODES	255	32	250
MEDIA	CATV COAX, FIBER OPTIC, TWISTED PAIR	TWISTED PAIR	TWISTED PAIR
ACCESS METHOD	TOKEN BUS	MASTER/SLAVE TOKEN	MASTER/SLAVE
SPEED BPS BITS/SEC	2.5M BPS	UP TO 10M BPS DEPENDING ON DISTANCES	2.4M/0.062M
HARDWARE COST PER NODE	$350	$80	$150

The cost/performance tradeoffs for selecting a network include topology flexibility, cabling requirements, data throughput, reliability, and ease of maintenance.

burg, OH). The chip set not only performs all of the lower level protocol tasks but also automatically reconfigures the network whenever a new node is activated or deactivated. And, since all Arcnet boards use the same chip set, you're assured that they can operate compatibly on the same network.

Arcnet is a token bus network that grants permission to talk only to the node holding the token. A node keeps the token for a maximum time limit before passing it to the next node. The time-limit feature makes it possible to calculate a worst-case time delay before a specific node can transmit on the network (see **box,** "Calculating the worst-case access time for Arcnet"). This deterministic quality of Arcnet makes it a good choice for real-time local networks. Remember, however, that a network only operates deterministically while it functions normally. Any induced noise or open connections that cause the COM9026 controller to reconfigure the network will degrade the network's performance.

To pass a message over the Arcnet network, a node must receive the token, verify that a receiving node is ready by transmitting a free buffer inquiry message followed by an acknowledge message from the receiving node, and transmit a data packet with cyclic redundancy check bits followed by an additional acknowledge message from the receiving node. Essentially five transmissions are involved: the token passing, the free buffer inquiry, the data packet, and the two acknowledge messages.

The Arcnet controller externally interfaces with 2k bytes of dual-ported RAM, which contains the data packets. The token passing, error detection, acknowledgments, and reconfigurations are automatically handled by the controller. Therefore, the interface software only has to manage the transmit- and receive-packet buffers and check the status registers for exceptions. The controller can generate an interrupt for each packet reception or transmission.

A packet can contain 1 to 252 bytes in short-packet mode and 255 to 508 bytes in long-packet mode. You can queue the data packets in the RAM buffer for transmission, but you must re-enable the controller after each transmission or reception. **Listing 2** outlines a program sequence in pseudocode for sending a block of data using the interrupt mode. Arcnet requires compatible routines on all communicating nodes, although other protocols may coexist on the network.

Arcnet boards are available for the STD Bus in various configurations. You can program them directly or use them in a PC-DOS-based system with a commercially available network package for an IBM PC-compatible computer. This technique facilitates communication between a computer and the STD Bus.

A short program is in session

Once you've chosen a local industrial network, you still must write the network software. Except in situations where fast response times or low unit costs are priorities, writing network software from the ground up is not usually necessary. If you write network software at a level that is independent of the hardware, you can shorten the development time.

Software written at the session layer of the OSI

Calculating the worst-cast access time for Arcnet

The one-way propagation delay of an Arcnet network can range from 0 to 31 μsec. Each byte transmitted over the network must be preceded by a start interval and followed by a stop interval, so that the total time to transmit a byte takes 11 clock intervals. Since Arcnet transmits at 2.5M bps, each byte requires 4.4 μsec to transmit. With a transmission overhead time of 141 μsec, the equation for the time to transmit a message is:

Message time = 141 μsec + 4.4 μsec × number of bytes in the data packet + 5 × propagation delay.

The time it takes to pass the token and send a data packet of one character with zero network propagation delay = 141 μsec + 4.4 μsec × 1 + 5 × 0 μsec = 145.4 μsec.

The time it takes to pass the token and send a data packet of 508 characters with the maximum network propagation delay = 141 μsec + 4.4 μsec × 508 + 5 × 31 μsec = 2531.2 μsec. Multiply these values by the number of nodes in the network. The worst-case access time for the token to circulate around the network falls between these two values.

(Open Systems Interconnection) model is independent of the network hardware; however, support for writing software at this level is not generally available for RS-422 and RS-485 networks. Mid-level implementations let you use commercially available installable device drivers to send messages to other nodes on the network. This approach is usually a proprietary nonportable solution and doesn't require a specific operating system.

An alternative mid-level approach is to use a common interface standard for both session and datagram communications. IBM's NETBIOS is one of many interface standards for PC-DOS computers. NETBIOS is installed as an extension to the computer's operating system **(Fig 2b)** and provides services for session-level communications between two nodes on a network as well as datagram support for broadcasts and communications between multiple nodes. The session-level commands are generally more efficient and reliable than datagrams.

The fastest way to implement the software, however, is to use a network package. These packages make transferring data across the network as simple as copying a file. A large variety of network packages that operate with various operating systems are available. Since PC-DOS is the most common operating system in use with the STD Bus, you'll want to consider the packages that run on this system. Novell's Advanced Netware and Western Digital's ViaNet are two representative examples.

With Netware one or more machines on the network acts as a file server. The servers are powerful machines with large disk capacities. Novell installs its own operating system on these machines to service requests from the network **(Fig 2c)**. The remaining machines, called workstations, use the file servers as a disk resource. This concept works well for database programs that require fast disk access to large amounts of data.

ViaNet is a distributed or "peer-to-peer" network where any machine on the network can share resources with any other machine. Communications proceed via the file system or through process-to-process facilities called pipes and sockets. ViaNet is not as fast as server-based systems for updating databases but is more flexible and fault tolerant.

Network software packages require at least 100k bytes of memory space and do not respond to requests as fast as the direct hardware-access approaches. But,

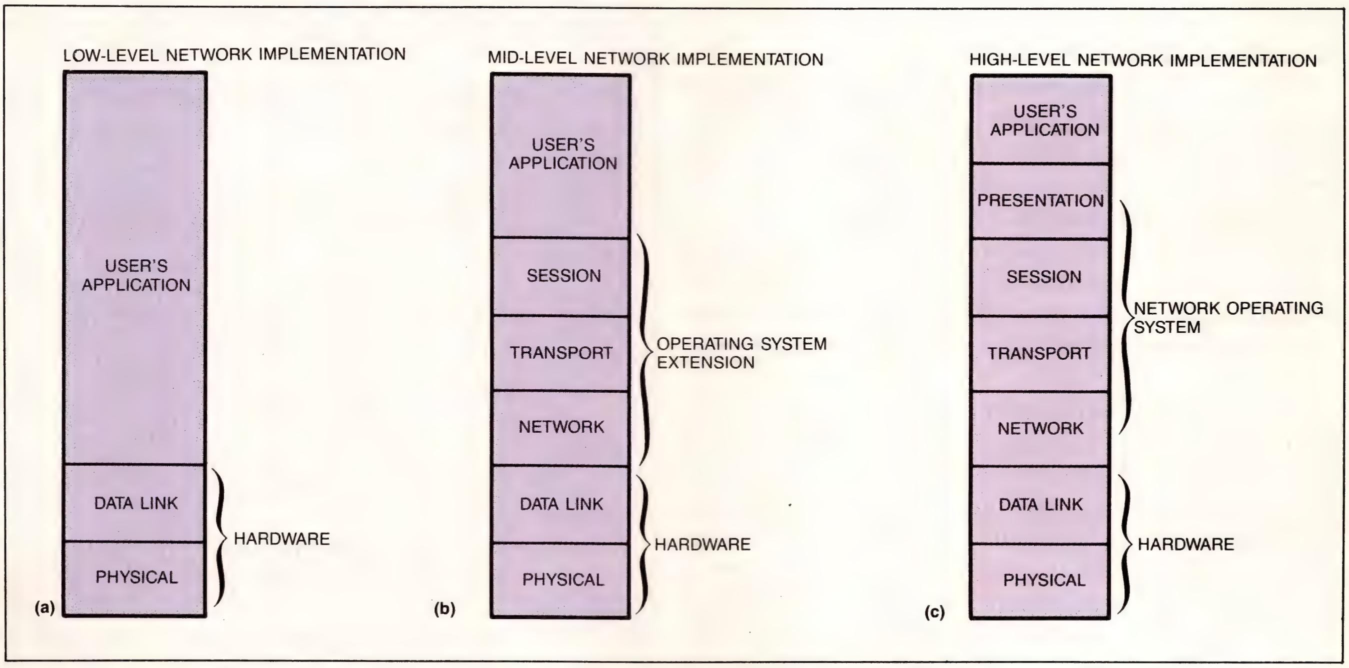

Fig 2—You can implement a local industrial network at different levels of the OSI (Open Systems Interconnection) model. *Commercially available ICs can execute the low-level protocols for low-level implementations, but an application program must perform the error detection and network routing tasks **(a)**. Mid-level implementations use extensions to the resident operating system to communicate over the network **(b)**. High-level implementations use network packages that include a network operating system **(c)**.*

You can realize a multipoint network with multiple drivers and receivers using the RS-485 standard.

they do let you develop software quickly by providing most of the complex network-management functions.

One of the disadvantages of PC-DOS network systems is that they are targeted at the personal-computer marketplace, which, by definition, has a user at every computer. Typical industrial-control applications have computers that are embedded machines. In fact, PC-DOS, when used in most STD Bus systems, does not implement keyboards or monitors, whereas IBM PC-compatible computers won't even boot without a keyboard connected. The designer must provide functions—such as program loading or termination, remote diagnostics, and possibly rebooting—to control remote embedded nodes.

Most PC-based networks provide remote file-access capability to each node on the network. The nodes can periodically retrieve control programs or log collected data to this common disk-storage unit, which can be located away from the harsh factory environment. A remote console is needed to operate embedded controllers on the network. Application programs on the embedded node need not worry about process-to-process communications. The programs simply input data from the Standard In port and output data to the Standard Out port. Thus, an operator or a control program can remotely operate a node anywhere on the network.

A remote-control implementation

Ziatech implements a Virtual Network Console (VNC) through a PC-DOS Terminate and Stay Resident program (TSR) and a PC-DOS installable device driver. The VNC program connects the console's Standard In and Standard Out ports to the network for control over the embedded units. It also provides a configurable transmission buffer for the data. The installable device driver provides a programmable interface to the remote supervisor program of each embedded node.

When a supervisor program wishes to send or read data to the remote console, it opens a device driver for the remote console. The device driver then places any written data into the queue for the Standard In port and retrieves any data in the Standard Out buffer. This operation is transparent to the embedded node. The node thinks it has a keyboard with a person typing at it and a terminal screen on which characters are appearing. The supervisor program begins at the DOS prompt when the program sends a path and program name to the remote console followed by a carriage return.

LISTING 2

```
Operating system considerations

Initialize the COM9026 Arcnet controller.
Enable interrupts from the controller.
Enable a page in the RAM buffer for data-packet storage.

IF the operating system needs to transmit a message.
   If the transmitter is available.
      Copy the message to a page in the RAM buffer.
      Set the destination-node address in the packet header.
      Set the message size in the packet header.
      Issue an Enable Transmit command.
   ELSE
      Set a transmitter-request flag for the Interrupt Service Routine.
   ENDIF
ENDIF

Arcnet controller Interrupt Service Routine

Check the status of the Arcnet controller.

IF a packet-received interrupt occurs.
   Copy the received packet from the RAM buffer.
   Notify the operating system of new data.
   Enable a page in the RAM buffer to receive the next packet.

ELSE IF a transmitter-available interrupt occurs.
   IF a message requires transmission.
      Copy the message to a page in the RAM buffer.
      Set the destination-node address in the packet header.
      Set the message size in the packet header.
      Issue an Enable Transmit command.
   ELSE
      Set transmit-available flag for the operating system.
   ENDIF
ENDIF
```

The Bitbus is an I/O network developed to overcome the problems associated with non-standard factory-floor communication links.

An example of a local industrial network illustrates some of the aforementioned considerations. **Fig 3** is a block diagram of a network connecting two complex control machines and a remote supervisory machine. The hardware configuration uses Arcnet in a multidrop configuration for each control machine. Both control machines are connected to an active hub, which is directly connected to the supervisory machine in a star arrangement.

Each of the control machines contains a machine-controller CPU that communicates with a number of individual task-controller CPUs. All of the CPUs run on an STD Bus using the PC-DOS operating system. Because of its topological flexiblity, speed, and reliability, Arcnet is well suited to this local industrial network. ViaNet network software provides the required distributed-network characteristics and an easy software platform for the programmer.

Since the task controllers are buried within the control machines, they don't require separate disks or an operator interface. These controllers have their operating-system and network software in EPROM. The machine controller loads the application task programs over the network; the control machines use the AUTOEXEC.BAT startup file to automatically load each program. Each task controller must store its configuration parameters, such as program identification variables, in local RAM. In addition, each task controller reports its results to the machine controller for storage in the machine's mass storage unit.

The machine controller provides the resources for the task controllers to load programs. It also processes the data received from each task and stores it for retrieval by the supervisory unit's CPU. If adjustments are required, the machine controller can alter the configuration parameters stored in the task controller's RAM.

The supervisory unit collects data, displays it on the

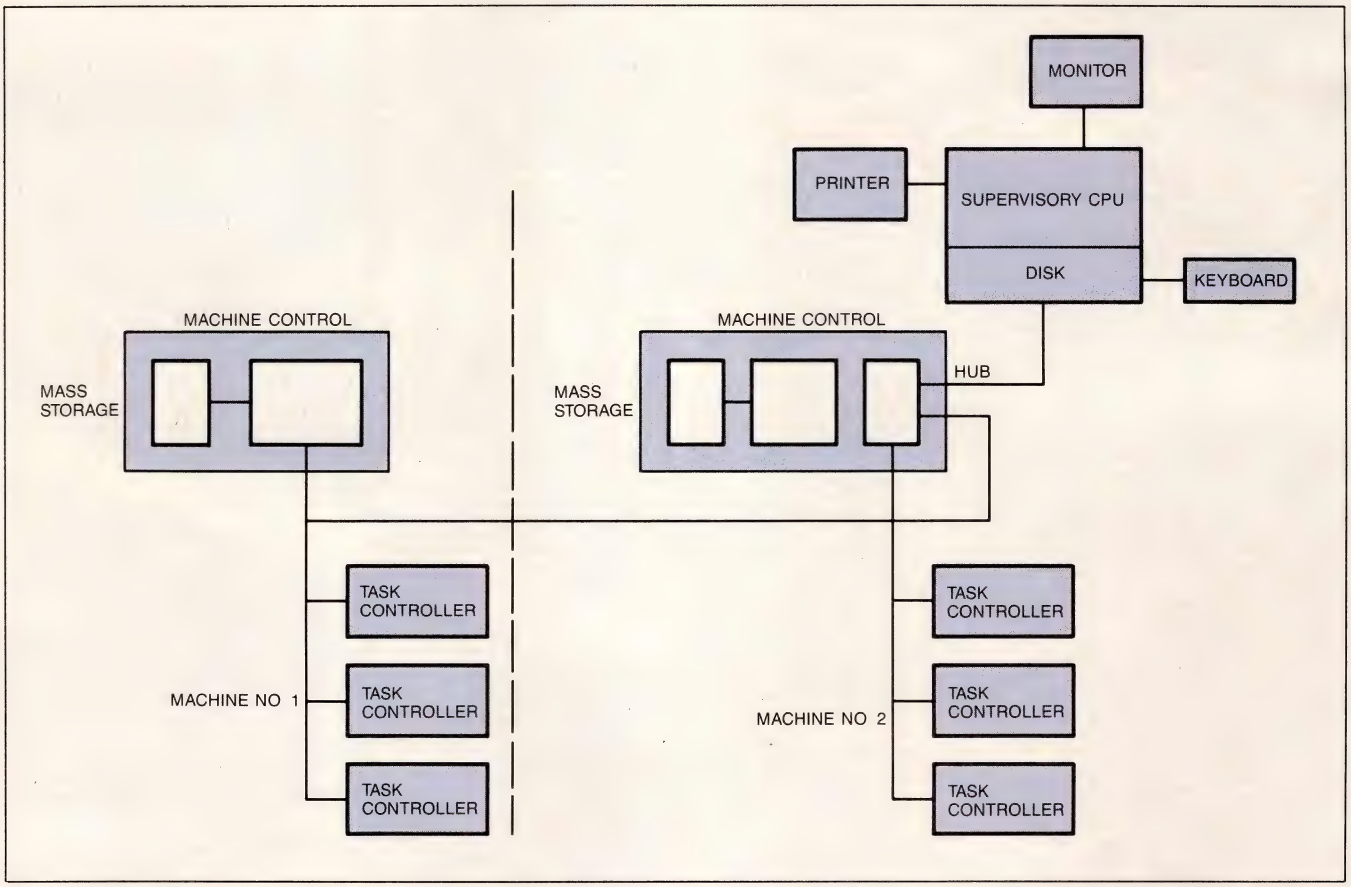

Fig 3—Local industrial topologies come in many shapes and sizes. *This example shows two complex machines with various task controllers operating from a machine controller via a multidrop configuration. Each machine communicates with a supervisory unit through an active hub in a star configuration.*

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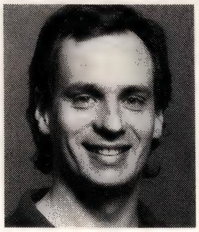
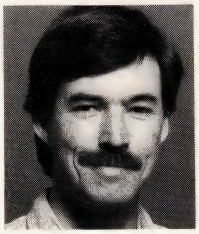
operator's console, and provides report-generation facilities. It also sends direct commands to the machine controllers through pipes at the session level. An operator at the supervisory unit can terminate the operation of any CPU and run diagnostics using the Virtual Network Console remote-control program. The supervisory unit can also implement gateway functions to another network, if necessary. EDN

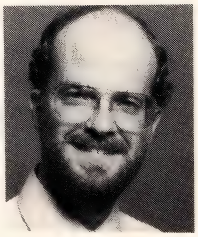
Authors' biographies



For the past year, Rob Davidson has been a product manager at Ziatech Corp. Previously he was employed by Honeywell Control Systems in Australia. Rob has a BSEE from Monash University in Melbourne, Australia.



As a software engineer at Ziatech Corp, Robert Metz is responsible for the system-level development of network and multitasking kernels. He was previously employed by Impell Pacific Corp, where he helped implement an Arcnet network with 800 nodes. Robert has a BSCS from California Polytechnic State University and is a member of the ACM SIGGRAPH special interest group on computer graphics. In his spare time, he enjoys gardening, woodworking, computer graphics, and music.



Alan Beverly is an engineering manager at Ziatech Corp. He has been with the company for nine years and is responsible for product planning, management, and direction. He graduated from California Polytechnic State University with a BS in electronics and holds one patent. He is a member of the IEEE and enjoys fishing in his spare time.

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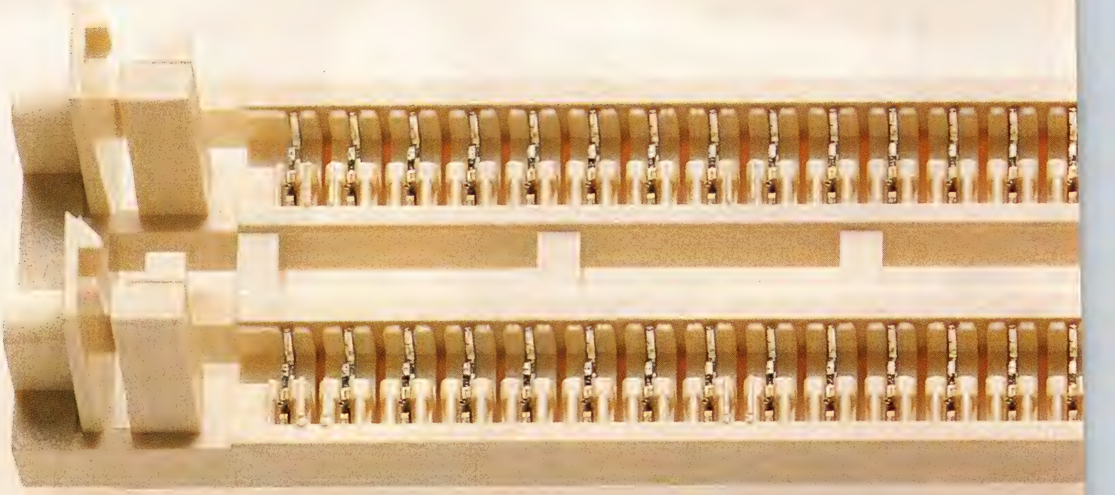

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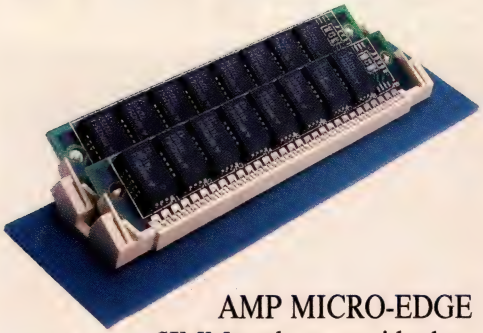

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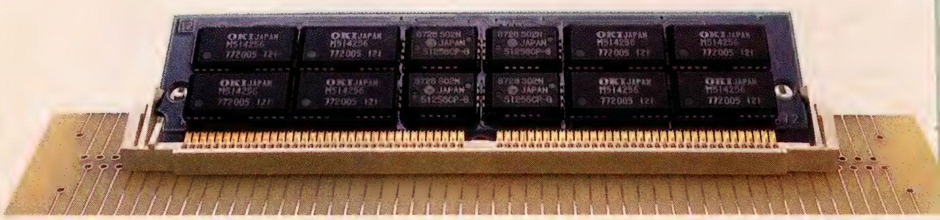

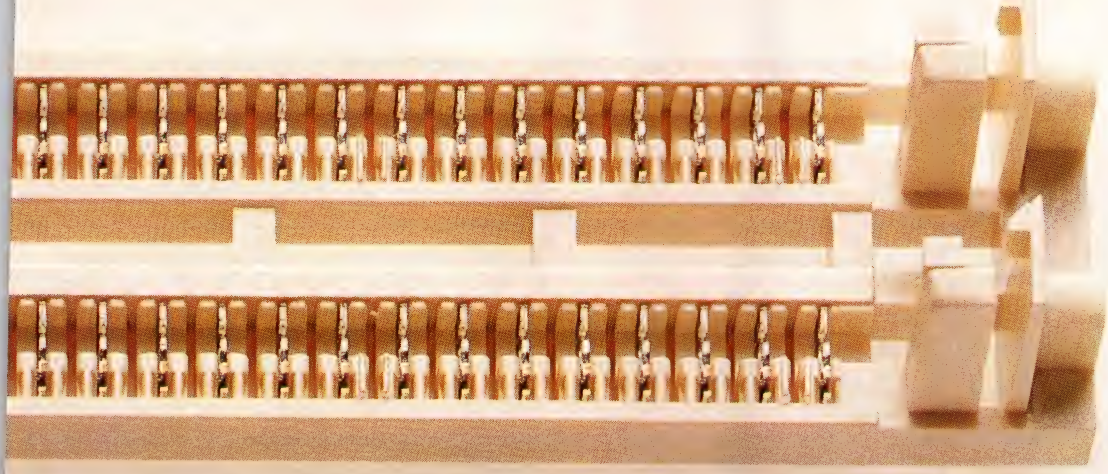

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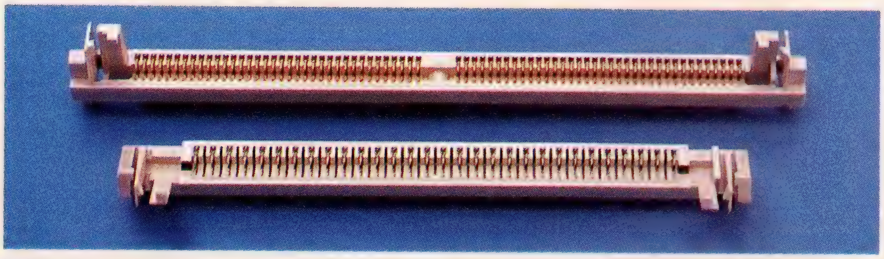

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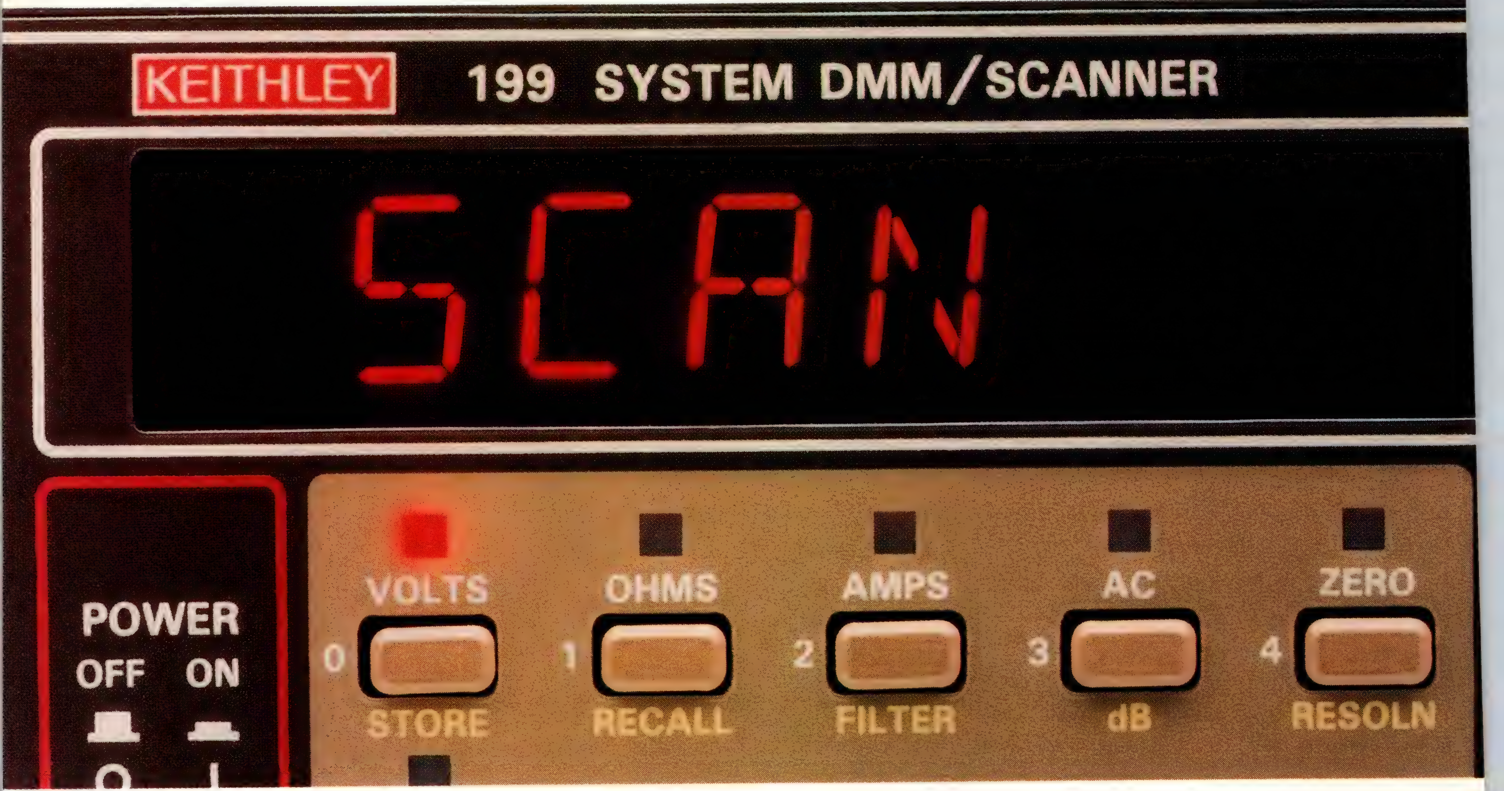

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EDITED BY CHARLES H SMALL

Thermal tester verifies transistors

Carlo Venditti
C S Draper Lab, Cambridge, MA

The tester in **Fig 1** verifies the thermal interface between a power transistor and its heat sink. The tester measures the temperature-sensitive V_{BE} of the transistor under test.

The tester first calibrates the dissipation of the transistor under test with a fixed, low-level current. Then it switches on a high current for a certain time and finally returns to the original low level. You record the V_{BE} at the various stages in this test to calculate the thermal resistance of the transistor/heat-sink interface.

To find the T_J max, first find the decrease in V_{BE} between the reading at the end of the high-power stage and the steady-state value during the low-power stage. Then, T_J°C = ambient temperature°C + decrease/2.2 mV/°C. Similarly, the effective total thermal resistance for the transistor/heat-sink assembly is (decrease/2.2 mV/°C) ÷ 10.

The tester uses an 11.4V input to yield 10W dissipation in the transistor under test. The tester comes up in the low-power mode; after warm-up, you can measure the low-level V_{BE}. When you press the test switch, the 555 timer turns on the DMOS switch, and the current in the transistor under test jumps to 1.1A. The timer times out in 2 minutes. You can use a variety of common lab instruments to record your data. EDN

To Vote For This Design, Circle No 746

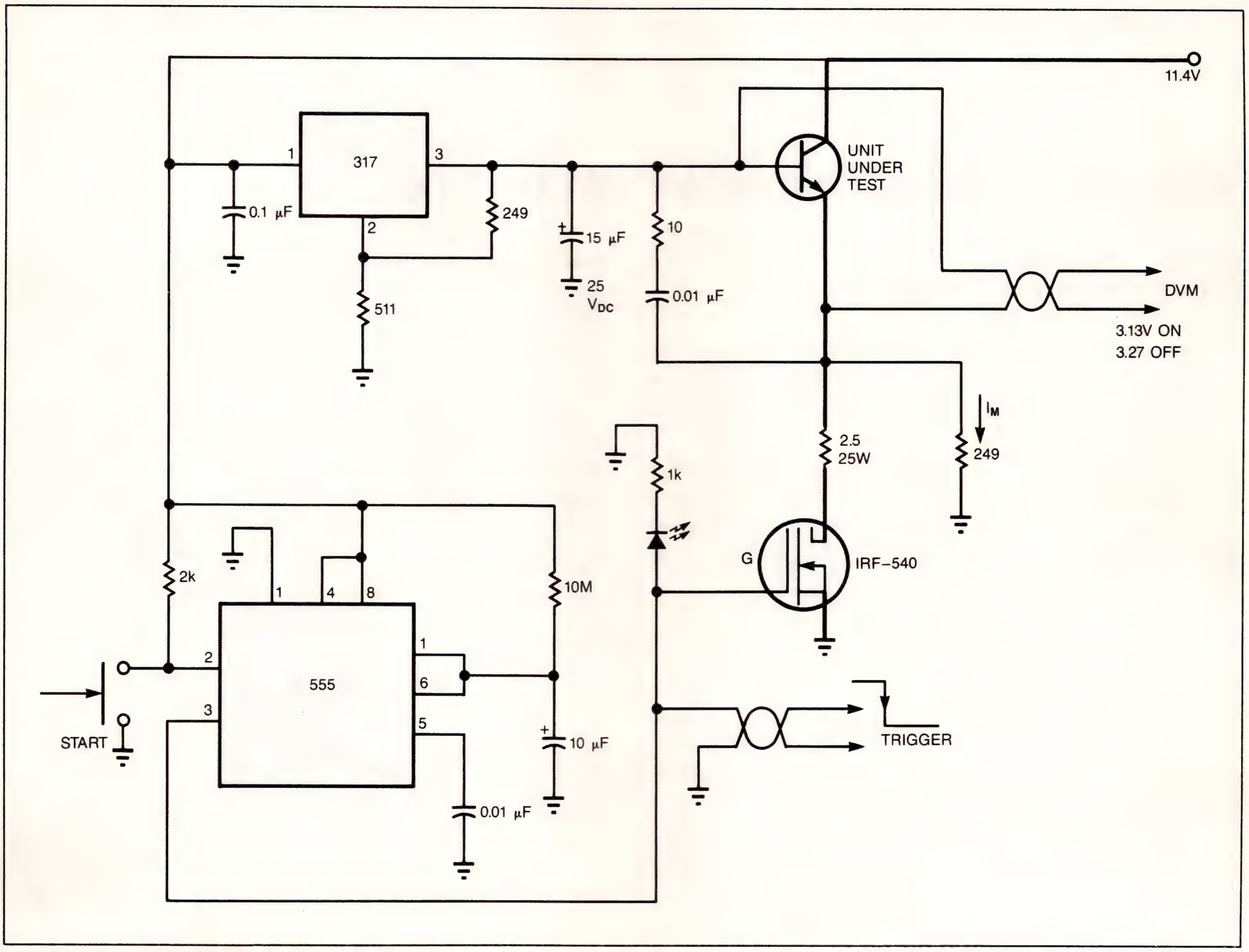

***Fig 1—This 10W thermal tester** applies a known high current to the transistor under test for a period of 2 minutes. You can calculate the thermal resistance of your transistor/heat-sink assembly from the change in V_{BE} you observe at high and low power levels.*

Single chip doubles frequency

James G Quigley
Boeing, Hill AFB, UT

The frequency doubler in **Fig 1** uses only one IC. Like other doublers, this circuit uses both the rising and falling edges of the input signal to produce digital pulses, thus effectively doubling the input's frequency.

Without the RC networks at IC_1 inputs, IC_1 would not produce any output pulses. However, the RC networks delay one edge with respect to the other. The A input lags the B input for positive-going edges, and the B input lags the A input for negative-going ones. You can vary the output duty cycle from 0 to 100% by varying R_3. IC_1's minimum output pulse width defines the maximum frequency of this circuit. EDN

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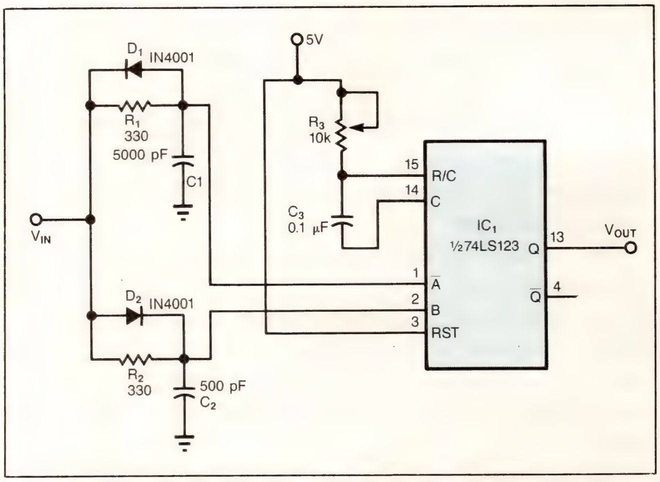

*Fig 1—**The RC-diode networks** at the inputs of the monostable multivibrator delay one edge with respect to the other. This action produces an output pulse for every input transition—positive or negative—effectively doubling the input frequency.*

Circuit modulates SAW oscillator

Michael A Wyatt
SSAvD Honeywell, Clearwater, FL

Adding a diode, resistor, and capacitor to the SAW (surface-acoustic-wave) oscillator in **Fig 1** allows you to use the oscillator in FSK (frequency-shift-keying) applications.

D_1, R_1, and C_1 form a simple diode switch in which D_1 shunts C_1 to ground. When the digital FSK input to R_1 is low, D_1 is off, and the small junction capacitance of D_1 couples C_1 to ground. A high FSK signal causes current to flow through R_1 and D_1. D_1's dynamic impedance is small when it is in forward conduction. Therefore, C_1 sees a lower-impedance path to ground. Thus the FSK input effectively switches C_1 in and out of the oscillator's circuit.

When C_1 is in the circuit (digital FSK is high), it pulls the frequency of the circuit to a slightly lower frequency because of the additional phase shift C_1 introduces at the GaAs FET's gate terminal (Dexcel, Div of Gould, Santa Clara, CA). The SAW device (RF Monolithics, Dallas, TX) restricts the amount of fre-

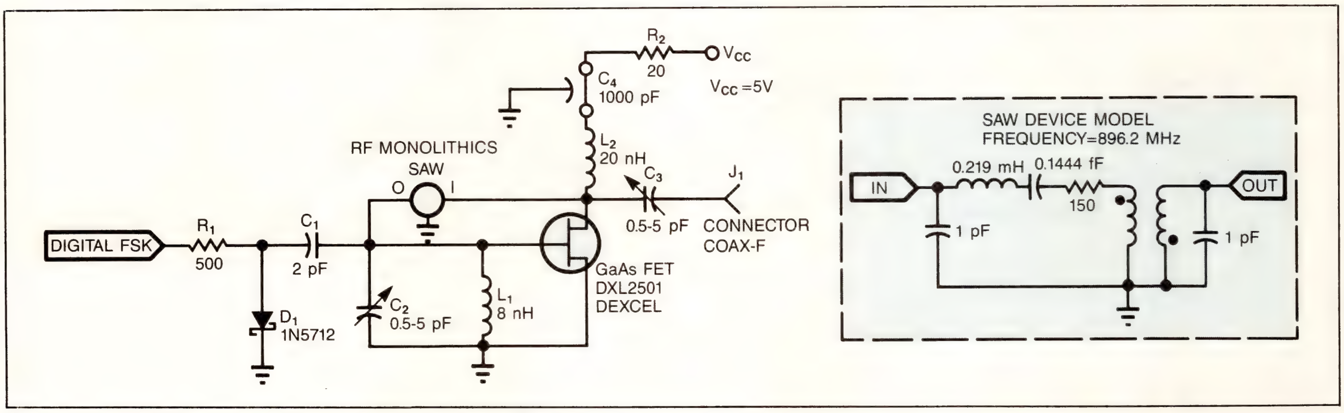

*Fig 1—**A simple RC-diode network** transforms a SAW oscillator into a FSK oscillator.*

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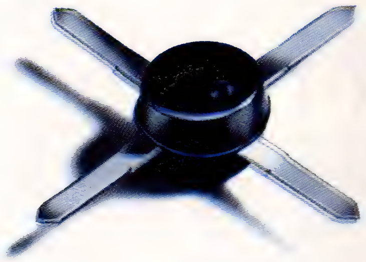

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MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
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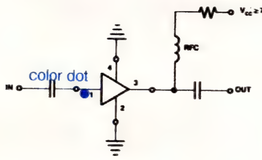

Also, for your design convenience, Mini-Circuits offers chip coupling capacitors at 12 cents each.†

Size (mils)	Tolerance	Temperature Characteristic	Value
80 × 50	5%	NPO	10, 22, 47, 68, 100, 470, 680, 100 pf
80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047. .068, .1μf

† Minimum Order 50 per Value

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C113-Rev. D

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quency shifting—usually less than 20 ppm for a high-Q SAW device.

The oscillator in **Fig 1** produces a center frequency of 896.2 MHz with an FSK deviation of 17 kHz when you drive the FSK input with a 0 to 5V signal. The frequency also depends on L_1 and C_2. EDN

To Vote For This Design, Circle No 747

JFET doubles isolator's bandwidth

Steven C Hageman
Calex Manufacturing Co, Pleasant Hill, CA

You must normally operate an optocoupler used in feedback loops at far below its −3-dB-gain frequency because the phase shift at this frequency is 45°—far too much for most feedback loops to tolerate.

The Miller effect is largely responsible for this limitation. Optoisolators like the CNY17-1 have a large junction-area photodiode connected between their collector and base. Because of this diode's large area, it has a large capacitance, which adds to the collector-base capacitance of the transistor—increasing the Miller effect.

One classical way to minimize the Miller effect is to minimize the collector-base voltage swing. The cascode-configuration using a JFET accomplishes this goal **(Fig 1)**. The cascode configuration presents an impedance of R_{DS} to the collector terminal of the optoisolator thereby reducing the voltage swing and increasing bandwidth. A $0.30 JFET such as the PN4393 in **Fig 1b** and **1d** can double the bandwidth of the CNY17-1.

Biasing for the JFET is essentially constant current because the optoisolator is within the feedback loop. Constant current biasing eliminates the effect of any JFET-parameter variation. And V_{GS} will set itself to whatever level is required for the given drain or emitter current. Thus you can select the JFET with the following constraints:

- I_{DSS} minimum must be less than the maximum expected drain or emitter current.
- The JFET must have a low R_{DS} (on) and moderate to low capacitance.
- The maximum signal swing will be reduced by the JFET's operating V_{GS}, so keep this reduction in mind.
- The JFET should have a low V_{GS} (off). EDN

To Vote For This Design, Circle No 750

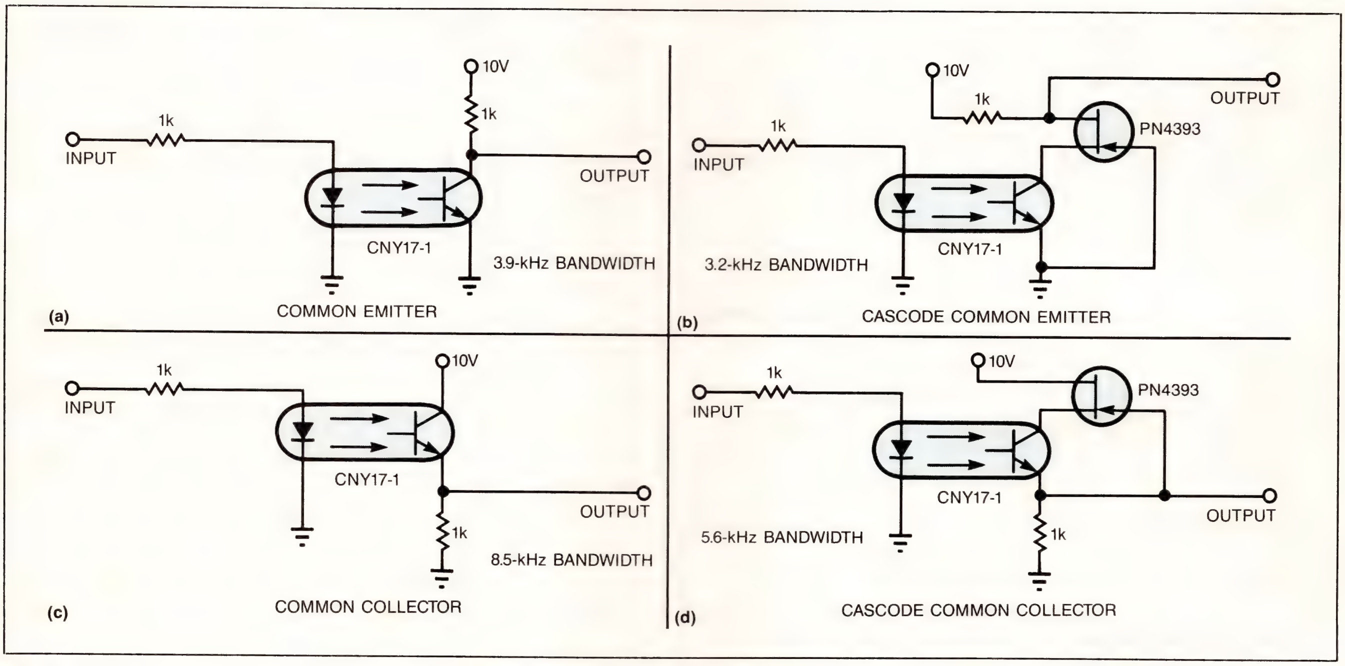


Fig 1—Adding a cascode stage to your optoisolator's *feedback elements can double the optoisolator's bandwidth.*

ISSUE WINNER

The winning Design Idea for the September 1, 1988, issue is entitled "Circuit lowers photodiode-amplifier noise," submitted by Rod Burt and R Mark Stitt of Burr-Brown (Tucson, AZ).

Your vote determines this issue's winner. All designs published win $100 cash. All issue winners receive an additional $100 and become eligible for the annual $1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

Fast algorithm divides big numbers

Man-Kit Lo
NCR Corp, Mountain View, CA

If you have some very large 64-bit numbers that you need to divide by a fixed number, conventional division algorithms could consume too much CPU time. Look-up tables won't work here either because a table of 64-bit numbers would be much too large.

Instead, you can use a method involving only addition. You first begin by building 16 small look-up tables. The tables correspond with each group of four binary digits (a HEX number) of the 64-digit multiplicand. Each table contains only 16 entries (for other than 64-bit numbers, you will have to adjust the number of tables). Each group of four bits (a HEX digit) of the multiplicand selects an entry from the one of the 16 tables that corresponds to that group. Each table entry selected by the 4-bit group holds a pair of results: the quotient of the hex digit of the multiplicand divided by the multiplier and the remainder of that division.

For example, for the 64-bit number (in HEX) $\mathrm{FECDBA9876543210}_{\mathrm{HEX}}$ divided by 20_{HEX}, the first table, corresponding to the left-most HEX digit, would have 16 entries. The entry corresponding to the $\mathrm{F}_{\mathrm{HEX}}$ would have two results: $\mathrm{F000000000000000}_{\mathrm{HEX}}$ divided by 20_{HEX} and the remainder of that division. The other 15 entries would contain similar pairs of results for $0000000000000000_{\mathrm{HEX}}$ through $\mathrm{E000000000000000}_{\mathrm{HEX}}$ divided by 20_{HEX}. The next table, corresponding to the next group of four binary digits (HEX digit) would have entries for $000000000000000_{\mathrm{HEX}}$ through $\mathrm{F00000000000000}_{\mathrm{HEX}}$ divided by 20_{HEX} and so on. Use this method until you have constructed 16 tables.

For each number you want to divide, use each group of four binary digits to select an entry from its corresponding table. Then sum all 16 remainders and sum all 16 quotients. The remainder sum must be less than $20_{\mathrm{HEX}} \times 16_{\mathrm{HEX}}$. You must then find the result of dividing this remainder sum by the divisor (you can use a look-up table having 320 entries in this example, or you could use the tables recursively). Finally you add the quotient of the original summing process to the quotient obtained from the division of the remainder. This sum is the final quotient. The remainder from the operation on the first remainder is the final remainder of the division. Got all that? EDN

To Vote For This Design, Circle No 749

If this is how you see LEDs, the ad is over.

The popular myth goes something like this: "An LED, is an LED, is an LED." Or: "If you've seen one, you've seen them all." And of course: "LEDs? They're commodity products."

Notions we at Dialight, steadfastly reject. And once you're familiar with our products, you'll know why.

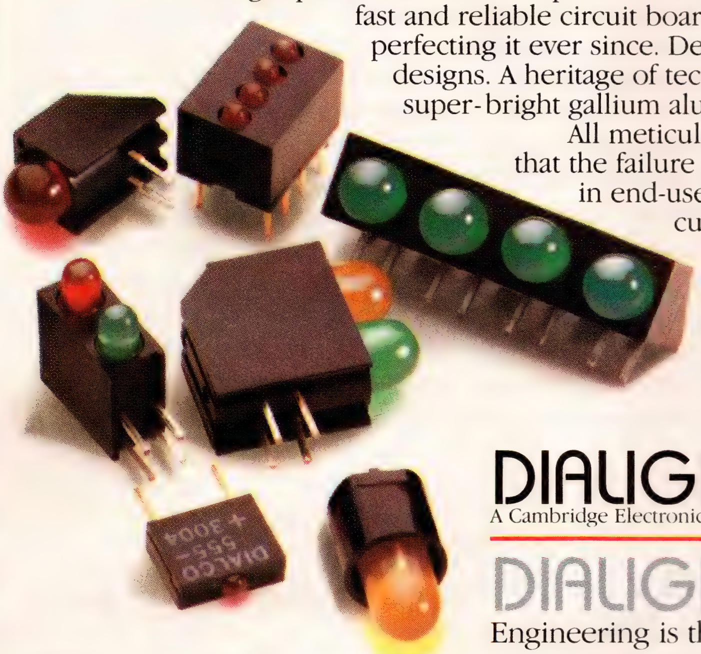
Take our Circuit Board Indicators. Single or multiple discretes aligned in a sturdy plastic housing, complete with their own current limiting resistor. The entire assembly polarity-keyed to guarantee correct insertion.

Each unit is 100% tested—ready to insert for wave soldering. No leads to bend, trim, or break. No time wasted fumbling with discretes.

Dialight pioneered the concept more than fifteen years ago to satisfy the OEM need for fast and reliable circuit board installation of LEDs. And we've been perfecting it ever since. Developing hundreds of standard and custom designs. A heritage of technological advance you can see in our new super-bright gallium aluminum arsenide units.

All meticulously engineered with the understanding that the failure of a "jelly bean product" can cost thousands in end-user downtime, and who-knows-what in customer loyalty.

The same understanding might bring you to call 201-223-9400, or write Dialight Corporation, 1913 Atlantic Ave., Manasquan, NJ 08736, and ask for our catalog or a product sample. At the very least, it's brought you to the real end of our ad.



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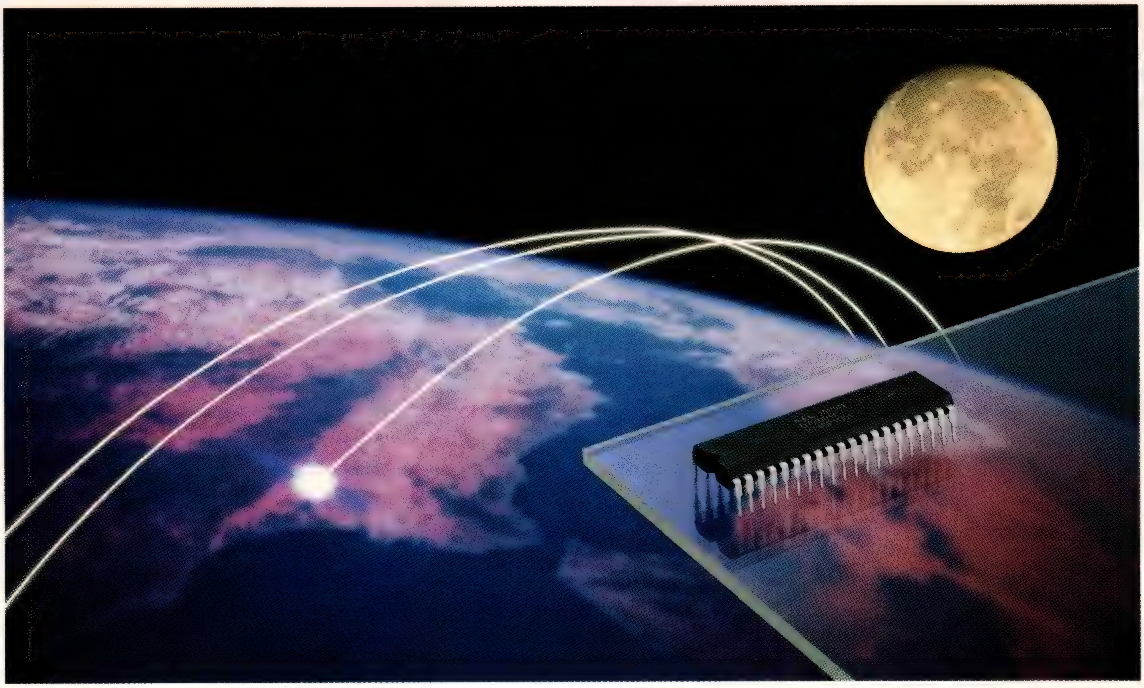

with NEC's multiprotocol serial controller.

The μPD72001 is an advanced CMOS multiprotocol serial controller that gives you extra flexibility and efficiency in data communications system design.

The μPD72001 is unique because it allows you to design a complex system with multiple transmit/receive speeds. The controller has two channels, a pair of transmit/receive blocks on each channel, and four independent on-chip baud-rate generators. You can use the baud-rate generators to set a different speed for each of the transmit/receive blocks.

The 72001 also supports an SDLC loop with on-chip hardware. It eliminates external control circuits to reduce host-CPU overhead. And it offers an on-chip DPLL (Digital Phase Lock Loop). The DPLL circuit reduces signal lines by picking up a clock frequency for control use from the data received in NRZI and FM formats.

Other features include a speed of 1.6M bits/sec.; asynchronous, COP, and BOP operations; and a standby function.

In today's fast-changing data communications universe, success depends on that extra margin of design flexibility. For the built-in versatility to meet diversifying user demands, design-in the μPD72001. Call us for full details today.

For fast answers, call us at:

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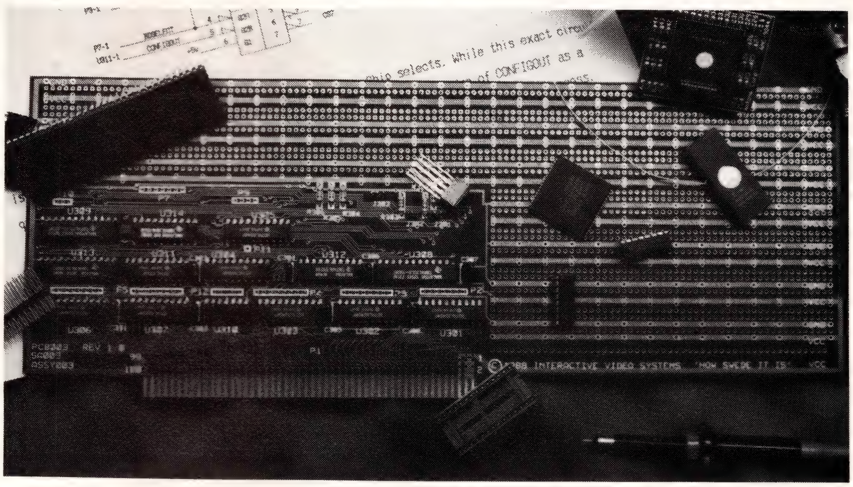
NEC

COMPUTERS & PERIPHERALS

PROTOTYPE BOARD

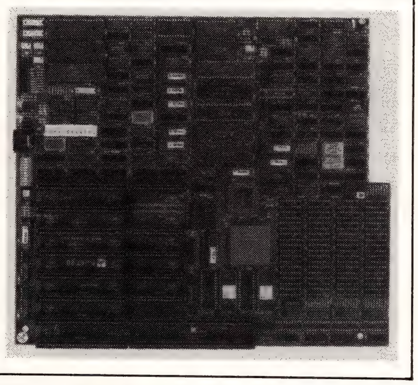
- *Develops expansion boards for the Amiga Computer*
- *Contains autoconfiguration logic for automatic installation*



The A2000 prototype board for the Amiga 2000 computer includes autoconfiguration logic for automatic system installation. The user can select from 1 to 31 wait states operating at 7 MHz, an address space ranging from 64k to 2M bytes, a link into a free memory pool, and interface-buffer direction control for any onboard DMA controllers. The buffers isolate the system bus from any onboard circuitry. The board's hole spacing accommodates ICs with 0.3, 0.4, 0.6, and 0.9-in.-wide pin spacing. It has a gridded ground structure and a V_{CC} bus, and can lodge as many as 44 16-pin ICs. It also includes headers and pads for DB9 and DB25 connectors. $139.95; a bare board without configuration logic, $59.95.

Interactive Video Systems, 15201 Santa Gertrudes Ave, Suite Y102, La Mirada, CA 90638. Phone (714) 994-4443.

Circle No 365



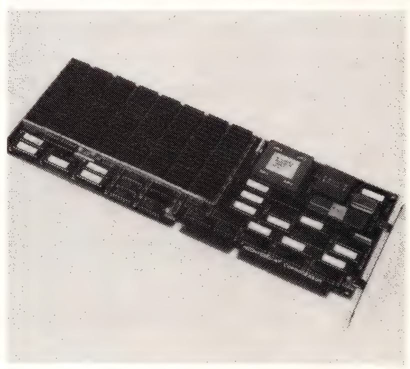
MOTHER BOARD

- *Has a 20-MHz 80386 μP and is IBM PC/AT compatible*
- *Has 1M byte of memory arranged in four banks of 256k-bit DRAMs*

The PEM-2000 IBM PC/AT-compatible mother board contains a 20-MHz 80386-20 μP that can be switched by software or hardware to operate at 8 MHz. The standard version has two serial ports and one parallel port. It also contains 1M byte of RAM arranged with four banks of 256k-bit dynamic RAMs having 80-nsec access times. The board has eight expansion slots: two 32-bit slots, five 16-bit slots, and one 8-bit slot. It also contains seven channels of DMA for disk and I/O access along with a 3-channel timer. A socket is available for an optional 20-MHz 80387 coprocessor. $1795.

DTK Computer Inc, 15711 E Valley Blvd, City of Industry, CA 91744. Phone (818) 333-7533. FAX 818-333-5429.

Circle No 366



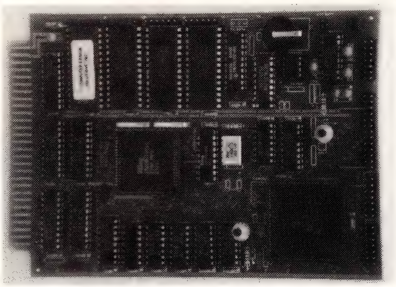
COPROCESSOR BOARD

- *Delivers 10 MIPS operating at 30 MHz for the IBM PC/AT*
- *Contains NS32532 CPU and 4M to 16M bytes of dynamic RAM*

The 532/AT coprocessor board for the IBM PC/AT computer contains an NS32532 CPU operating at 25 or 30 MHz. The board has 4M bytes of dynamic RAM, which can be expanded to 16M bytes with an optional daughter board. The 532/AT board can run Unix and DOS applications simultaneously. In addition, the board supports Ready Systems VRTX and Genix V.3 operating systems. When operating at 30 MHz, the board delivers from 8 to 10 VAX 11/780 MIPS. "Bus master" functions within the board permit the operation of as many as four coprocessors in parallel in the same enclosure. The board typically draws 4A from the 5V supply and operates from 0 to 35°C with 0 to 95% humidity. An optional NS32381 floating-point processor is also available. Board with optional floating-point unit, $9980.

Aeon Technologies Corp, 90 S Wadsworth Blvd, Suite 105-481, Lakewood, CO 80226. Phone (303) 777-6142.

Circle No 367



STD CPU BOARD

- *Uses the Z280 μP and is compatible with Z80 object code*
- *It includes as much as 128k bytes of ROM or battery-backed RAM*

The H280STD CPU board for the STD Bus uses the Z280 μP. Because the μP is compatible with the object code for the Z80 μP, it can run Z80 applications including CP/M. In addition, it can take advantage of the Z280's onboard cache, 24-bit address space, memory management, and hardware multiply-and-divide circuitry. It includes as much as 128k bytes of ROM or of battery-backed RAM in any combination. The board comes with three RS-232C ports and a 20-bit parallel I/O port. The board also has eight counter/timers for real-time process control. $395.

Computer Design Solutions Inc, Box 127, Statesville, NC 28677. Phone (704) 876-2346. FAX 704-872-7103.

Circle No 368

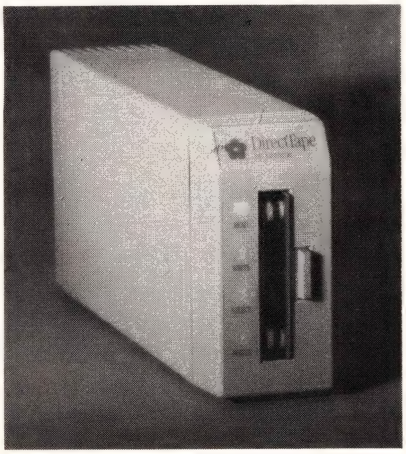
9600 BPS MODEM

- *Designed for interactive file-transfer applications*
- *Transmits at 9600 bps in one direction and 1200 bps in the other*

Designed for interactive file-transfer applications, the FDX 9624 full-duplex 9600-bps modem is compatible with CCITT V.22bis, Bell 212A, and Bell 103 modem specifications. Based on the CCITT recommendation V.32, the modem transmits data at 9600 bps in one direction and 1200 bps in the other without using echo-cancellation techniques. It operates over the public switched telephone network (PSTN) or over leased lines. It uses a combination of MNP Class 4 adaptive data compression and Trellis-coded modulation to transmit data. In addition, MNP Class 5 compression increases the speed to more than 17,000 bps. Other features include automatic fall-back and fall-forward capabilities, tone or pulse dialing, a nonvolatile memory for storing configurations, automatic voice-to-data switching, and auto-dialing. The Hayes-compatible modem costs $899.

Fastcomm Communications Corp, 12347-E Sunrise Valley Dr, Reston, VA 22091. Phone (800) 521-2496; in VA, (703) 620-3900.

Circle No 369



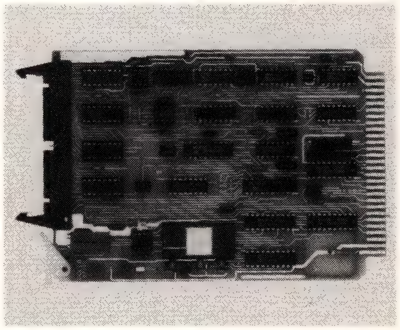
TAPE DRIVE

- *Backs up a 40M-byte disk in 16 minutes*
- *Uses QIC-100 recording format*

The DirectTape 40M-byte tape drive for Macintosh computer users employs DC2000 ¼-in. data cartridges and the QIC-100 recording format. Designed for the SCSI bus, the drive is compatible with Apple Computer's Tape Drive 40SC and the AppleShare network. The system can handle data from any tape originated on an Apple computer. The drive can do image backups at 2.5M bytes/minute and file-by-file backups at 2M bytes/minute. It can back up a 40M-byte SCSI hard-disk drive in 16 minutes and automatically verify the data. Other features include icon software, a background formatting utility, the ability to mark files and folders, and a T-connector for easy connection. $1099.

Jasmine Technologies Inc, 1740 Army St, San Francisco, CA 94124. Phone (415) 282-1111. FAX 415-648-1625.

Circle No 370



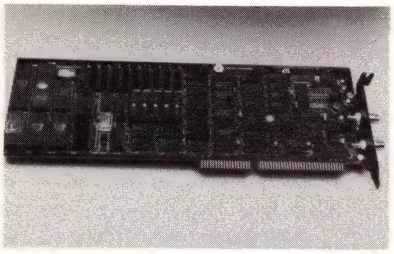
STD A/D CARD

- *Features 32 single-ended inputs to a 12-bit A/D converter*
- *The converter has a linearity spec of ±½ LSB*

The AD-1232 A/D converter card for the STD Bus features 32 single-ended or 16 double-ended input channels to the converter. The ADC has a 12-bit resolution, a linearity of ±½ LSB, a maximum conversion time of 25 μsec, and a 25-kHz throughput rate. A programmable conversion mode converts from 12- to 8-bit operation for faster conversion rates. A continuous conversion mode allows continuous sampling of one of the channels, thereby allowing data to be always available without waiting for a conversion completion. Another special mode makes the card compatible with Analog Devices' RTI-1260 A/D card. The board doesn't contain dc to dc converters and requires ±12 to 15V from the STD Bus power supply. $495.

XYZ Electronics Inc, Rural Rte 12, Box 322, Indianapolis, IN 47236. Phone (800) 852-6822; in IN, (317) 335-2128.

Circle No 371



INTERFACE BOARD

- *Emulates NTDS specified in MIL-STD-1397 Type D.*
- *Implements a 10M bps communication link between nodes*

The Navigator Model NT32D IBM AT-type interface board emulates Navy Tactical Data Systems (NTDS) as specified in MIL-STD-1397 Type D. It supports the Type D high-speed serial-communications scheme that replaces the 192-wire parallel-communications link with two 75Ω serial coaxial links. It emulates three NTDS nodes: MIL standard host computers; peripheral units including fire control and electronic counter measure radar units; and auxiliary computers to communicate with the host. The board also provides a 10M-bps serial link between nodes. The board contains BNC connectors for each of the serial links. A built-in test feature disconnects the serial link from the BNC connector and loops the signal to the input for diagnostic tests. Three programmable timers update independent bogey displays to emulate approaching vessels or aircraft. $4950. Delivery, four to six weeks ARO.

Sabtech Industries Inc, 3910-B Prospect Ave, Yorba Linda, CA 92686. Phone (714) 524-3299.

Circle No 372

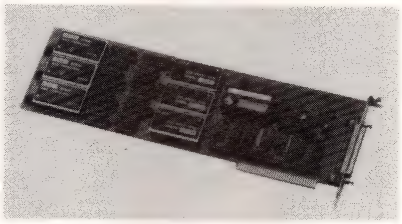
COMPUTER

- *Runs an 80286 μP at 20 MHz*
- *Expandable to 8M bytes of memory on the mother board*

The 20-MHz 80286 μP in the AMT-286/25 IBM PC/AT-compatible computer runs programs from zero-wait-state RAM to achieve a performance that's claimed to exceed that of many 80386-based machines. Performance is further improved when the computer is fitted with Harris Corp's optimized 80286 μP. Peripheral circuitry is based on Chips and Technologies' Neat chip set. Features of the board include separately selectable numbers of wait states for I/O ports, 8- and 16-bit DMA transfers and the processor bus; selectable clock speeds; interleaved or noninterleaved RAM paging; LIMS/EMS memory expansion beyond the 640k-byte limit imposed by DOS; and shadow RAM that allows you to run the BIOS from RAM. The mother board can accept as much as 8M bytes of RAM. Version with a monochrome monitor, 40M-byte hard disk, and 1.2M-byte floppy disk, £2145.

Applied Microsystems Technology Ltd, 249-251 Cricklewood Broadway, London NW2 6NX, UK. Phone 01-450-3222. TLX 94016308. FAX 01-452-0738.

Circle No 373



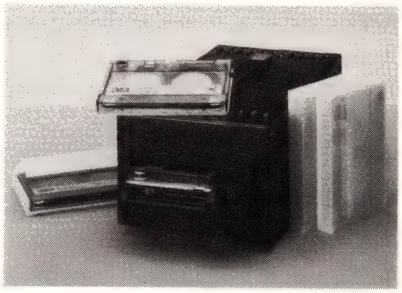
CONVERTER CARD

- *Provides R/D and S/D functions for the IBM PC bus*
- *Models with 1 to 6 channels have an accuracy of ±1.3 minutes/arc*

The SDC-36015 IBM PC card contains from one to six channels of resolver-to-digital and synchro-to-digital conversion. The card uses either a DDC RDC-19200 hybrid circuit for resolver inputs or a DDC SDC-14560 hybrid circuit for synchro inputs. The converters have jumper-programmable resolutions of 10, 12, 14, or 16 bits. The card has an accuracy specification of ±1.3 minutes/arc and provides two 8-bit data words to the computer for angle data. In addition, the board provides 4 bits for counting the number of turns, built-in test data, and loss-of-signal data for each channel. All the digital information is memory mapped to four RAM locations to be read by the host. The card's operating temperature range is from −55 to +125°C. From $1095. Delivery, stock to 12 weeks.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 310-685-2203. FAX 516-567-7358.

Circle No 374



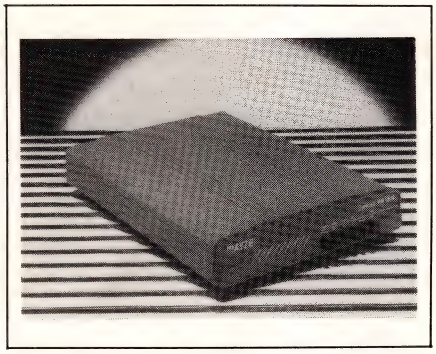
TAPE STREAMER

- *Provides a portable tape backup system*
- *Includes drivers for the OS-9 operating system*

Housed in a portable case and provided with its own power supply and SCSI interface, the VME 68812-ST streamer provides a backup capacity of 60M bytes or 155M bytes on DC600A 1/4-in. tape cartridges. The streamer connects to the host system via a 50-way ribbon cable. The unit comes with software drivers for the OS-9 operating system. Using the OS-9 utilities FSAVE and FRESTORE, you can archive complete file systems or back up hard disks on tape. You can also configure the backup operations as background tasks to minimize system interruption. 60M-byte version, DM 4280.

EKF Elektronik GmbH, Weidekampstrasse 1a, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621. FAX (02381) 15067.

Circle No 375



MODEM

- *Allows dial-up communications at 4800 bps*
- *Has autodial and autoanswer facilities*

The Syncro-48-Dial modem allows you to use synchronous dial-up communications links at 4800 bps. The modem uses the half-duplex CCITT V.27-ter 4800-bps transmission technique, and is suitable for applications such as microcomputer to mainframe, and point-of-sale communications, where fast response is required. Autodial and autoanswer facilities are included as standard, and an integral speaker allows you to monitor call progress. A separate command port allows you to control the modem without disturbing the main data channel. In addition, the modem has 12 preset modem configurations, which you can select by operating front-panel push buttons. The Syncro-48-Dial modem is fully compatible with the company's other Syncro-48 modems. £595.

Mayze Systems Ltd, Delta 900, Great Western Way, Swindon, Wiltshire SN5 7XQ, UK. Phone (0793) 511789. TLX 445707. FAX (0793) 511683.

Circle No 376

CPU CARD

- *Its 68020 processor runs at speeds between 12 and 25 MHz*
- *Suitable for multiprocessor environments*

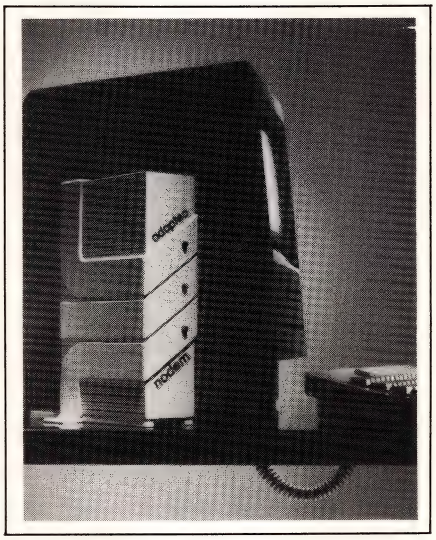
The VMPM68KC-2 single-Eurocard VME Bus CPU card runs a 68020 µP and an optional 68881 or 68882 floating-point math coprocessor. The 68020 processor can run at speeds between 12 and 25 MHz. The board has 1M byte of onboard dual-port RAM and a real-time clock. A lithium-cell battery provides backup for both the RAM and the real-time clock. The board's interrupt logic makes it suitable for use in multiprocessor environments, and the interrupt handler allows you to mask interrupts at each interrupt level. The board is available for operation in the industrial or extended temperature ranges. DM 2400.

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 81001. TLX 541233. FAX (08341) 40422.

Circle No 377

Pep Modular Computers Inc, Carnegie Office Park, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 378



LAN INTERFACE

- *Connects SCSI-based computers to Ethernet networks*
- *Accepts Appletalk network data unmodified*

The Nodem interface unit connects all SCSI-based computers to Ethernet and Cheapernet networks. The unit comes in an external box that measures 5×8×2 in. and plugs directly into a SCSI port. When operating with Macintosh computers, it accepts Appletalk network data unmodified. It operates transparent to the computer user. Essentially, it expands the 32 nodes of Appletalk's physical media, LocalTalk, to the 254 nodes of Ethernet and the 230k-bps communications rate of LocalTalk to the 10M-bps rate of Ethernet. To accommodate different Ethernet options, you can insert a snap-in media card in the box to permit communications over twisted-pair lines. An Ethernet version, $545; Cheapernet and twisted-pair versions, $595.

Adaptec Inc, 691 S Milpitas Blvd, Milptitas, CA 95035. Phone (408) 945-2520.

Circle No 379

LAN BOARD

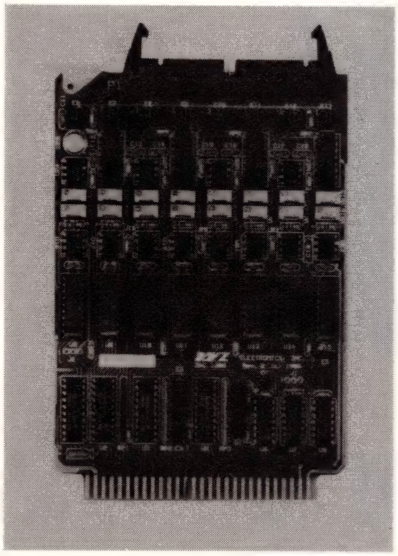
- *Interfaces to Ethernet or Cheapernet LANs*
- *Has an onboard 68000 µP for protocol and data processing*

The VME68570-LAN double-Eurocard VME Bus board provides an intelligent interface to IEEE-802.3 networks. The board's LAN interface has a transceiver for direct connection to a Cheapernet LAN, and a 15-pin D-connector attachment unit interface (AUI) for connection to an Ethernet transceiver. A 7990 LAN controller that transfers data using DMA to or from 512k bytes of onboard RAM controls these LAN interfaces. An onboard 12.5-MHz 68HC000 µP allows you to process the data locally before passing it to the VME Bus host system. The board operates as a VME Bus slave, communicating with the VME Bus host via 2k bytes of onboard dual-port RAM and inter-

rupts or semaphores. As an alternative, you can install as much as 128k bytes of EPROM and use the board as a stand-alone system. Software drivers to implement the TCP/IP protocol are available for the OS-9 operating system. DM 2650.

EKF-Elektronik GmbH, Weidekampstrasse 1a, 4700 Hamm 1, West Germany. Phone (02381) 12630. TLX 828621. FAX (02381) 15067.

Circle No 380

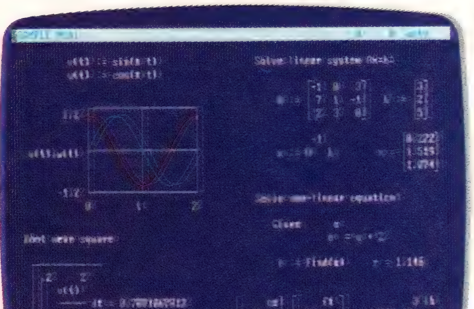


DAC CARD

- *Has eight separate DACs for the STD Bus*
- *Each converter has 12-bit resolution with ±½-LSB linearity*

The DAC-1208 D/A converter card for the STD Bus places eight individually addressable D/A converters on one card. Each converter offers 12-bit resolution with ±½-LSB linearity and guaranteed monotonicity. Each channel is user selectable for bipolar or unipolar operation with output ranges as large as ±10V. The user can select an internal or an external reference for each channel. The internal reference is 10V. When an external reference is supplied, the card can act as a digitally controlled attenuator for signals as large as ±10V. You can order the unit with less than eight

Your pad or ours?



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Requires IBM PC® or compatible, 512KB RAM, graphics card.

IBM PC® International Business Machines Corporation.
MathCAD® MathSoft, Inc.

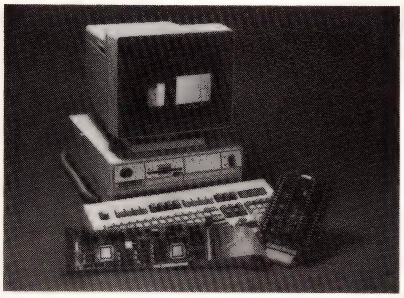
MathCAD®

MathSoft, Inc., One Kendall Sq., Cambridge, MA 02139

channels and 8-bit resolution DACs at lower cost. Card with eight 12-bit channels, $595.

XYZ Electronics Inc, Rural Route #12, Box 322, Indianapolis, IN 47236. Phone (800) 852-6822; in IN, (317) 335-2128.

Circle No 381



ACQUISITION BOARDS

- *For the IBM PS/2 models 50, 60, and 80 computers*
- *Each board has a 50-kHz ADC with 12-bit resolution*

1The DT2901 and the DT2905 are data-acquisition boards for the IBM PS/2 models 50, 60, and 80 computers. Each board contains a 50-kHz A/D converter for 16 single-ended or 8 double-ended inputs. The DT2901 has software-selectable gains of 1, 2, 4, 8, and 16; the DT2905 has gain settings of 1, 2, 10, 20, 100, 200, 500, and 1000. Each board has two independent 12-bit D/A converters operating at 50 kHz and 16 digital I/O lines that can operate while inputting analog data. Two custom ICs control the onboard data transfers and interfaces to the Micro Channel bus. The boards have a set of features designed to eliminate data gaps. An error-detection circuit and two DMA channels define two data buffers in system memory that can be chained together to prevent data loss. DT2901, $895; DT2905, $995.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. TLX 951646. FAX 508-481-8620.

Circle No 382

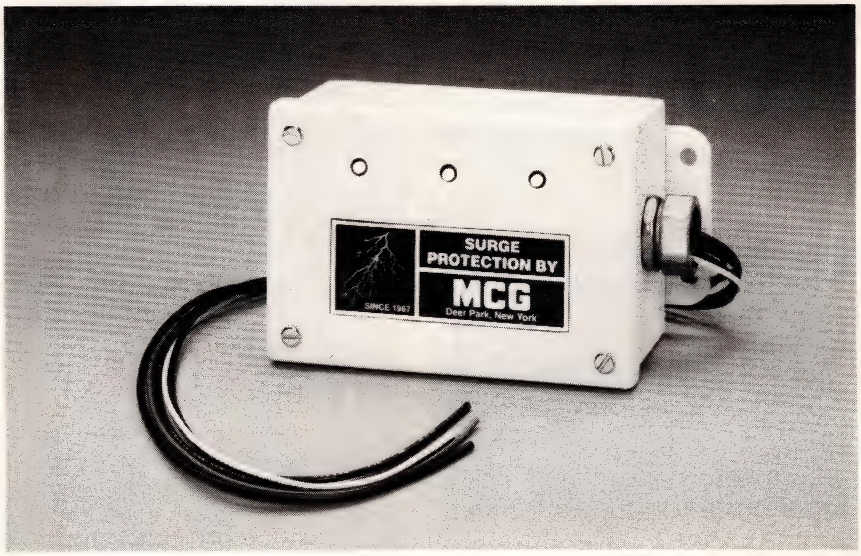
NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

SUPPRESSORS

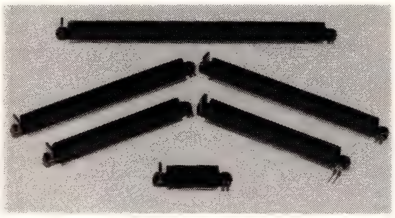
- *Have a 5-nsec response time*
- *Recover automatically without power interruption*

SPA Series transient suppressors react in 5 nsec to transients that appear on ac power lines. The units install at the local service panel (load side with rating ranging to 50A), and shunt the power lines they are protecting. They employ parallel metal oxide varistors on each phase and UL-listed components throughout. After each transient, the SPA units recover automatically without power interruption. Three front-panel LEDs indicate that protection is present on each phase. Models are available for voltages of 120, 208, 240, 277, or 480V. Single-phase, wye, and delta-power configurations are available. From $355.



MCG Electronics Inc, 12 Burt Dr, Deer Park, NY 11729. Phone (516) 586-5125. TLX 645518.

Circle No 405



CONNECTORS

- *Feature zero insertion force*
- *Offer as many as 320 contact positions*

Designed for zero insertion force, BetaFlex connectors integrate shape-memory-alloy (SMA) and flexible-circuit technology. The 22 models in the family have centerline spacings ranging from 0.025 to 0.1 in. They are stackable and modular and feature a contact density ranging as high as 80 contacts/in. The leads, contacts, and electrical connections within the housings are all incorporated in a polyimide flexible circuit. The contact areas are selectively plated with gold over a nickel underlayer. The connectors are surface-mount designed. The traces in the connectors are pressed against the traces on the board. A simple low-voltage power supply within the housing opens the SMA element. After inserting the daughter board, you remove power and the contacts close. The electrical life is rated for 500 open/close cycles min. $0.23 per contact.

Beta Phase Inc, 1060 Marsh Rd, Menlo Park, CA 94025. Phone (415) 494-8410.

Circle No 406

KEYLOCK SWITCHES

- *Available in 1- or 2-pole versions*
- *Life span exceeds 25,000 rotations at low current*

Series 500 rotary keylock switches offer as many as six tumblers and are available in 1- and 2-pole versions. Providing as many as 12 positions, the switches have an operating life of 25,000 rotations at low current. The sealed explosion-proof switches have a solid detent feel with indexing at 30, 36, 45, and 90°. The switches provide 5-disk keying, and 6-disk keying is available as an option. The dry-circuit switches are compatible with solder-lug or pc-board type terminals. Terminal contacts are silver alloy crown on copper alloy and are gold plated. $8.50 to $13 (1000). Delivery, 12 weeks ARO.

Oak Switch Systems Inc, Box 517, Crystal Lake, IL 60014. Phone (815) 459-5000.

Circle No 407

TRIACS

- *Operate without snubber networks*
- *Available with a range of gate sensitivities*

The BTA06 and BTA08 triacs are available with gate sensitivities of 35, 50, or 75 mA. Current ratings for the devices are 6A and 8A, respectively. In most applications, their switching performance and immunity to switching spikes allow you to use them without snubber circuits. Versions are available with peak off-state voltages between ±200 and ±700V. The minimum

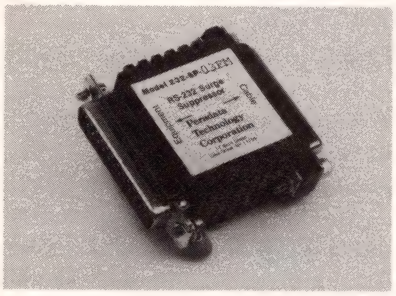
commutation parameters (dV/dt) for the 35, 50, and 75-mA sensitivity devices are 250, 500, and 750 V/μsec, respectively. Corresponding minimum parameters $(dI/dt)_c$ for the BTA06 are 3.5, 5, and 8A/msec, and 4.5, 7, or 10A/msec, respectively, for the BTA08. These $(dI/dt)_c$ values are specified at the maximum junction temperature of 125°C and without snubber networks. The triacs are housed in plastic TO-220 packages. BTA06, approximately \$0.65; BTA08, approximately \$0.75 (1000).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 408

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 409



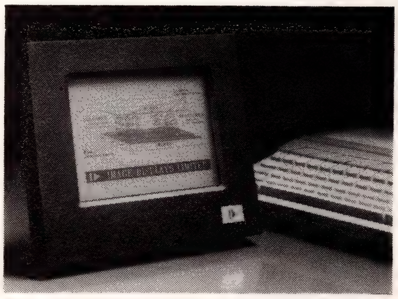
SUPPRESSOR

- *Designed for RS-232C data lines*
- *Features a 3-stage suppression network*

The Model 232-SP in-line surge suppressor is designed to protect RS-232C data lines in demanding industrial applications. The unit features a proprietary 3-stage surge-suppression network, which provides subnanosecond response. The 232-SP has a 25V max let-through voltage, tested to IEEE Standard 587 with a 6000V, 100 kHz, 500A ring wave. Models are available configured as gender changers, null modem adapters, and printer adapters. The suppressor measures $2.2 \times 1.9 \times 0.7$ in. and comes with standard 25-pin connectors. From \$29.50.

Peradata Technology Corp, 17 Birch St, Lake Grove, NY 11755. Phone (516) 588-2216.

Circle No 410



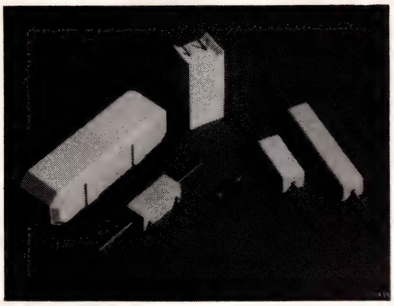
FLAT-PANEL DISPLAY

- *Provides ink-on-paper readability*
- *Requires no refreshing*

According to the manufacturer, these electronically addressed smectic liquid-crystal displays provide high-resolution flicker-free displays that are readable in bright ambient light conditions and have a viewing angle equivalent to that of ink-on-paper printed material. Once updated, the displays do not require any refreshing, thereby eliminating the requirement for high-speed drive circuitry and providing a high degree of data security. You can update the entire screen of a 640×480-pixel display in less than 300 msec. The displays are initially being manufactured as 4-, 8-, and 14-in. diagonal versions. The 14-in. version can display a full-size A4 page. The initial displays are black and white, but color versions are under development. Samples of the 640×480-pixel display, complete with interface circuitry and a power supply, are available for £600. In high volume, the displays will compete in price with supertwist LCD technologies.

Image Displays Ltd, Maypole Corner, London Rd, Harlow, Essex CM17 9NA, UK. Phone (0279) 443344.

Circle No 411



RESISTORS

- *Designed for surface mounting*
- *Power ratings range to 50W*

All wirewound power resistors in these six lines are designed for surface-mount applications. Type WS units feature power ratings to 3W with tolerances of ±0.25 to ±5%. The general-purpose units in the WX, WR, and WU families feature power ratings ranging from 2 to 50W and standard tolerances of ±5 and ±10%. Type WE power low-resistance wirewound and Type WF 4-terminal resistors feature resistance values as low as 0.005Ω. Standard power ratings range from 3 to 15W and tolerance specifications equal ±1 to ±10%. Bulk or tape-and-reel packaging is available. $0.07 to $1.12 (1000). Delivery, stock to 12 weeks ARO.

Allen-Bradley Co, 1414 Allen-Bradley Dr, El Paso, TX 79936. Phone (800) 592-4888; in TX (800) 292-4888.

Circle No 412

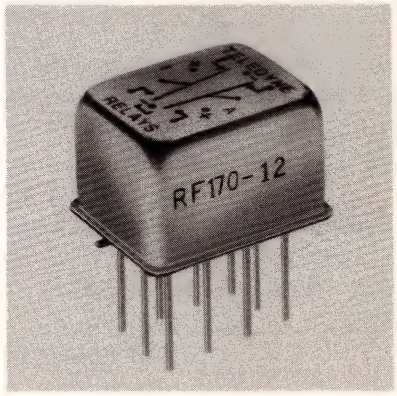
CHIP INDUCTORS

- *Designed for trouble-free handling in placement equipment*
- *Operate to 105°C*

IMC-1812 Series chip inductors feature inductance values of 0.01 to 1000 μH. They are available in a moisture-resistant molded package that's compatible with vapor-phase and infrared soldering methods and features a tapered design for problem-free handling in automatic placement equipment. Solid phosphor-bronze terminals eliminate leaching problems. Standard tolerance is ±20% over a 0.01- to 0.39-μH range and ±10% for 0.47- to 1000-μH inductances. Tolerances of ±5 and ±3% are also available on request. The inductors operate over a −20 to +105°C range and are normally supplied in tape-and-reel packaging. $0.35 (1000). Delivery, stock to eight weeks ARO.

Dale Electronics Inc, E Highway 50, Yankton, SD 57078. Phone (605) 665-9301.

Circle No 413



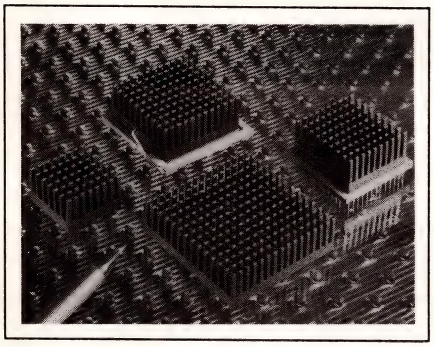
RF RELAY

- *Features low intercontact capacitance*
- *Designed for applications with density problems*

With a low-profile height and 0.10-in. grid spacing, the commercial-grade RF170 suits applications requiring high packaging density and/or close pc-board spacing. The hermetically sealed, magnetic-latching device features low intercontact capacitance for high performance over the entire VHF/UHF spectrum. At 1 GHz, isolation across the contacts equals 42 dB, insertion loss measures 0.19 dB, and VSWR is 1.2. At 3 GHz, respective figures are 33 dB, 0.3 dB, and 1.5. The relay operates with a short-duration pulse input. No holding power is required after the contacts transfer, thereby providing a nonvolatile memory capability. $38.80 (100).

Teledyne Relays, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. FAX 213-779-9161.

Circle No 414



HEAT SINK

- *Designed to cool pin-grid arrays*
- *Suited for impingement-cooling applications*

The 2334 pin-fin heat sink is designed for 21×21-position pin-grid arrays (PGA). The unit is suited for impingement cooling where the airflow is ducted directly into the fins—perpendicular to the mounting surface. The pin-fin design can improve thermal performance by as much as 20%, when compared to extruded heat sinks of similar volume. The heat sink measures 0.65 in. tall and has a thermal resistance of 2.1°C/W with a 400-ft/min airflow. You can use the heat sink with the company's PGA E-Z Mount assembly, or you can bond it with epoxy to the PGA. The mounting assembly eliminates thermal expansion mismatch problems and provides a secure mechanical attachment between the heat sink and the PGA. $0.65 (1000).

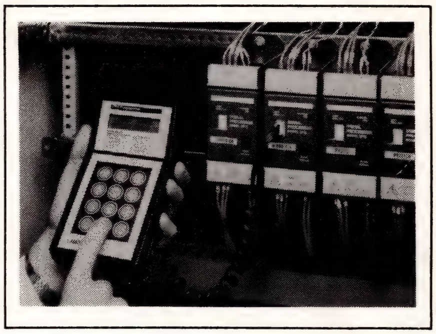
Thermalloy Inc, Box 810839, Dallas, TX 75381. Phone (214) 243-4321. FAX 214-241-4656. TLX 203965.

Circle No 415

I/O MODULES

- *Accept a range of industrial process control inputs*
- *Programmable via a handheld programming unit*

The Sapphire range of signal-conditioning modules is µP controlled, allowing you to program the units to accept a range of input signals. You carry out programming operations with the aid of a plug-in programming unit. The Model SP10 accepts thermocouple inputs or other low-level input signals. It provides thermocouple linearization to BS-4937 standards for six thermocouple types and accepts low-level input ranges as high as ±65 mV. The Model SP20 accepts platinum resistance thermometer inputs and linearizes them to BS-1904. In addition, you can use it to measure re-



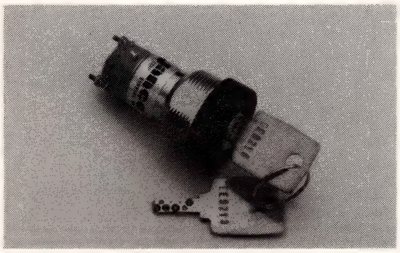
sistances as high as 5 kΩ, using a 3-wire measurement technique that eliminates cabling errors. The Model SP30 provides general process control inputs—for example, 4- to 20-mA or 1 to 5V signals. It provides a loop power-supply facility, impedance matching, and front-end signal processing functions that include exponential, logarithmic, or linear scaling. In addition to their analog inputs, all the modules feature alarm and control outputs, and an analog output with current or voltage output options. SP10 £275; programming unit, £275.

Protech Instruments & Systems Ltd, 241 Selbourne Rd, Luton, Bedfordshire LU4 8NP, UK. Phone (0582) 596181. TLX 825274. FAX (0582) 598808.

Circle No 416

Rotork Controls Inc, 19 Jet View Dr, Rochester, NY 14624. Phone (716) 328-1550. FAX 716-328-5848.

Circle No 417



KEYLOCK SWITCHES

- *Feature unitized construction*
- *Can carry 10A*

Series BKS rotary keylock switches feature a totally enclosed, explosion-proof, unitized construction that exceeds the requirements of MIL-STD-3786. Most models in the line can carry currents ranging to 10A. The switches are available with indexings of 30, 36, 45, 60, and 90°. Position capability ranges from 2 to 12 in a choice of 1, 2, and 3 poles per deck. The units can switch 250 mA resistive at 28V dc or 115V ac, and 120 mA inductive at 28V dc. The lifetime is 10,000 cycles, and the operating range spans −65 to +125°C. A BKP Series pc-board-mountable version is also available. $65 (100). Delivery, eight to 10 weeks ARO.

Janco Corp, 3111 Winona Ave, Burbank, CA 91504. Phone (818) 846-1800. TWX 910-498-2701. FAX 848-842-2296.

Circle No 418

TRANSCEIVER

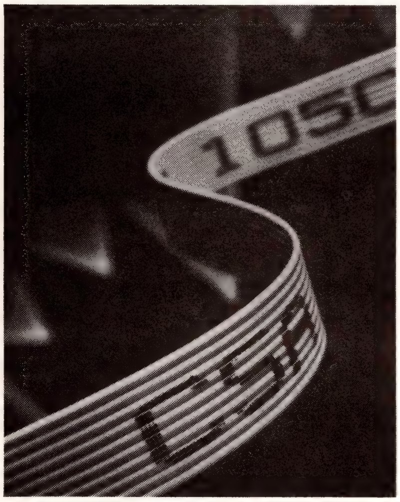
- *Provides access to Ethernet*
- *Contains a diagnostic test function*

The RL3000 coax transceiver provides access to Ethernet LANs for transmitting and receiving data. Fully compatible with IEEE 802.3 and Ethernet version 2.0 specifications, the transceiver provides a

signal quality error (SQE) or heartbeat test function, which is customer or site selectable to meet the requirements of specific Ethernet devices. It also features LED indicators for power, transmit, receive data, and collision detect. The transceiver is available with stinger or N-type connectors for attachment to standard 10Base5 Ethernet cable or with BNC-type connectors for 10Base2 Ethernet cable. $249 (OEM qty).

Siecor Electro-Optic Products, Box 13625, Research Triangle Park, NC 27709. Phone (919) 481-5100.

Circle No 419



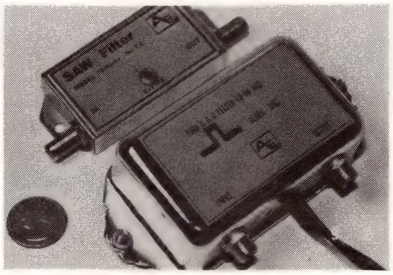
FLAT CABLE

- *Available with 9 to 64 conductors*
- *Features CSA approval*

Series 9L280XX flat cable has from 9 to 64 #28 AWG stranded conductors spaced on 0.05-in. centers. Approved by the CSA for wiring applications in the Canadian market, the cable features a gray PVC jacket and a red stripe for easy polarity identification. Designed for easy termination from either the top or bottom, you can also easily slit the cable for breakouts where more than one connector is required at an end. The cable meets all IEEE-802.3 and CCITT X.21 specifications and is recommended for EIA RS-422 applications. Series 9L cable is available in 100- and 300-ft put-ups. $19.73 to $449.87.

Belden Wire & Cable, Box 1980, Richmond, IN 47375. Phone (800) 235-3364.

Circle No 420



BANDPASS FILTERS

- *Feature built-in amplifiers*
- *Provide high out-of-band attenuation*

Designed for use in TV-receive-only receivers, these surface-acoustic-wave TVRO bandpass filters insert a high loss for out-of-band frequencies—60 dB outside the 60- to 80-MHz range. The Model 70-Micro filter includes input and output buffer amplifiers. The gain equals 1 dB. Powered by 18V from the through-power on the coaxial cable, it draws only 50 mA. The 70R filter, similar to the 70-Micro but slightly larger, includes a built-in remote-controlled switch, which allows you to remove the switch from the system electronically. $100.

Alaun Engineering, 2305 Florencita Dr, Montrose, CA 91020. Phone (818) 957-0618.

Circle No 421

LOG AMPLIFIER

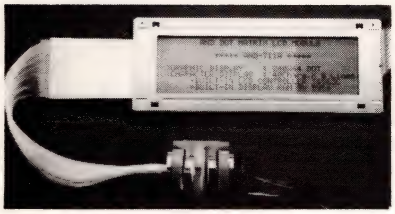
- *Features an 80-dB dynamic range*
- *Has a 200-nsec rise time*

The ICLP2105 IC log amplifier operates at 21.4 MHz and has a 5-MHz bandwidth. It features a full 80-dB dynamic range (−80 to 0 dBm) and offers ±0.5-dB linearity measured at 25°C. A 200-nsec rise time makes the amplifier suitable for both continuous-wave and communications-

system applications. The units are available with power connectors for those applications where solder-on leads are not suitable. An RFI-shielded compartment is provided for the connector and the interconnections. Standard amplifiers operate from ±12V dc supplies and draw 85 mA. Units are available for ±15V dc operation. $1450. Delivery, 90 days ARO.

RHG Electronics Laboratory Inc, 161 E Industry Ct, Deer Park, NY 11729. Phone (516) 242-1100. TWX (510) 227-6083. FAX 516-242-1222.

Circle No 422



LIGHTING PANELS

- *Feature easy installation*
- *Have 17,000-hour lifetimes*

Enhanced readability, dc white light, and long life are some of the major features of these fiber-optic backlights. The units are light-emitting panels woven from acrylic optical fibers. Computer-controlled micro-bends cause the transmitted light to exceed the critical angle of the fiber's core-cladding interface, allowing the light to leave the fiber without damaging the cladding surface. The panel's light source is a 2.5W halogen lamp that is aligned in a reflector assembly for maximum light transfer to the fibers. All infrared and ultraviolet energy is filtered out at the source. The average lamp life at 4.5V is 17,000 hours. $19 (100) for a panel that backlights a 240×60-pixel super-twist LCD dot-matrix module.

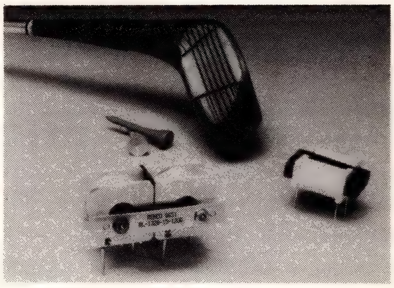
AND, 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916. TLX 6771439. FAX 415-340-1670.

Circle No 423

CHOKES

- *35A current ratings*
- *Windings balanced within 1%*

Series RL 1328 and 1329 common-mode chokes are designed to suppress transient noise from feeding back into power lines. When the units are installed in the equipment power-line input, the inductively coupled, out-of-phase windings ef-



fectively cancel any transients. Over 200 standard models are available with current ratings ranging to 35A. Choke windings are balanced within 1%. All units are high potential tested, winding to winding and winding to core, at 2500V ac. The operating range spans −55 to +130°C. The chokes meet UL, CSA, and VDE specifications; MIL-spec and encapsulated units are also available. From $2.50 (1000). Delivery, stock to eight weeks ARO.

Renco Electronics Inc, 60 Jefryn Blvd E, Deer Park, NY 11729. Phone (516) 586-5566. FAX 516-586-5562.

Circle No 424

INDUCTORS

- *Handle 35A currents*
- *Come in pc-board-mountable packages*

Offering a wide range of inductance values, IHB Series chokes are available in pc-board-mountable packages. The six models in the line cover a 1 to 47,000 μH inductance range. DC resistance measures from 0.002 to 6.19Ω. Current ratings equal 0.8 to 35A. The chokes are available with standard tolerances of ±10 and ±20%. All units come with pretinned 0.5-in.-long leads; insulated coverings are available as an option. 1-μH, ±20% tolerance choke, $2.55 (500). Delivery, stock to eight weeks ARO.

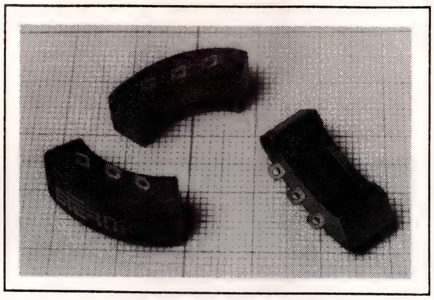
Dale Electronics Inc, 1122 23rd St, Columbus, NE 68601. Phone (605) 665-9301.

Circle No 425

POSITION SENSOR

- *Measures angular displacement*
- *Resistant to shock and vibration*

These angular position sensors allow you to detect angular displacements between ±20 and ±30°. Other angular-displacement versions are available as custom devices. They have a resistive track and are suitable for applications



that must withstand high levels of vibration. They are also insensitive to shock and high acceleration forces. The devices operate over a temperature range of −55 to +125 °C. They weigh 1.5g and are housed in 20×10×7-mm packages, which form a quadrant of a circle. $25 (1000).

Sfernice, 199 Blvd de la Madeleine, 06021 Nice Cedex, France. Phone 93446262. TLX 470261. FAX 93862726.

Circle No 426

Ohmtek, 2160 Liberty Dr, Niagara Falls, NY 14304. Phone (716) 283-4025. TWX 710-524-1653. FAX (716) 283-5932.

Circle No 427

HEADERS

- *Conserve board real estate*
- *Offer 20- to 128-pin capacity per stacked assembly*

The Condo right-angle, latch-and-eject, boxed header system stacks the connectors vertically to save board real estate. Individual headers are available in 10- to 64-position versions, providing a 20- to 128-pin capacity per stacked assembly. The units are compatible with 0.1-in. flat-cable/connector harnesses and standard IDC (insulation displacement connector) sockets. The headers have 0.155-in. solder tails located on a 0.1×0.1-in. pc-board grid. $12.01 (1000) for a 50-position unit. Delivery, four to six weeks ARO.

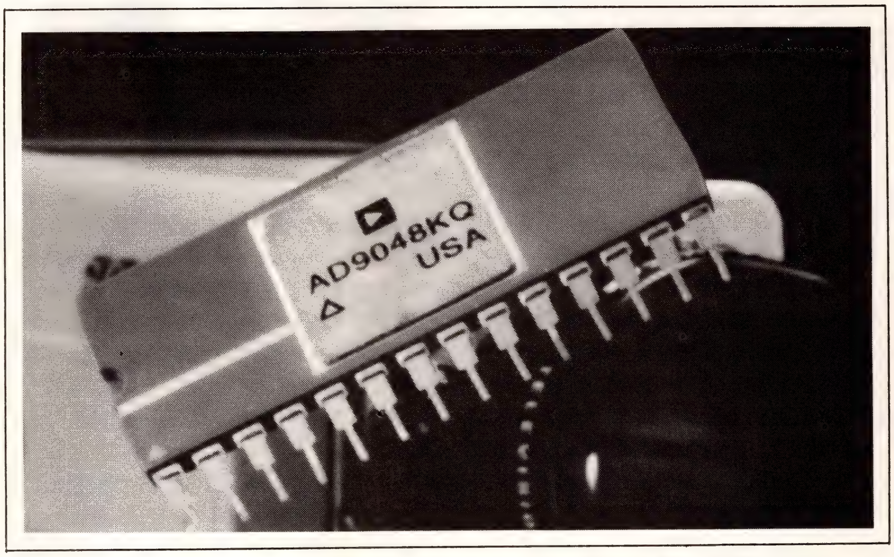
3M, Dept 3P27, Box 2963, Austin, TX 78769. Phone (512) 834-1800.

Circle No 428

INTEGRATED CIRCUITS

8-BIT FLASH ADC

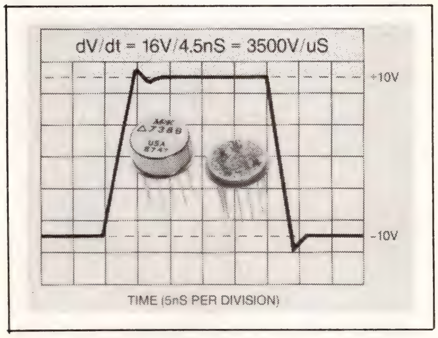
- *10-MHz input bandwidth*
- *35M-sample/sec conversion rate*



Offered as an improved alternate source to the TDC-1048, the AD9048 8-bit flash A/D converter features a 10-MHz input bandwidth and a minimum conversion rate of 35M samples/sec without degrading the S/N ratio or dynamic performance. The converter's low input capacitance of 16 pF reduces analog phase shifts and the drive requirements of an input buffer amplifier. The maximum differential and integral nonlinearity is ¾ LSB, increasing to 1 LSB over temperature. With 1.248-MHz and 9.35-MHz inputs, the corresponding rms S/N ratios are typically 44 dB and 40.5 dB. After a full-scale step, the AD9048's settling time to 8-bit accuracy is 20 nsec max. The typical recovery time after a −3V overvoltage input is 8 nsec. The AD9048 dissipates 550 mW and operates from 5V and −5.2V supplies. Several package options, temperature grades, and accuracy grades are available. From $20 (100). Delivery, four to six weeks ARO.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 351



PRECISION OP AMP

- *3500V/µsec slew rate*
- *20-MHz full-power bandwidth*

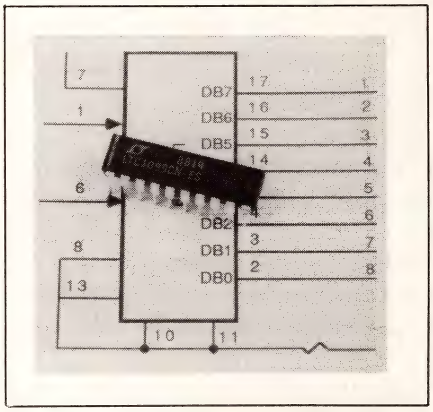
Using a feed-forward design topology along with RF bipolar transistors and thin-film input resistors, the MSK-738 op amp achieves both precision and high speed. The device's specifications include a slew rate of 3500V/µsec and a full-power bandwidth of 20 MHz, both guaranteed minimums at its full-rated output of ±10V into a 100Ω load. For a 10V step under its rated load, the MSK-738 settles to 0.1% in 30 nsec. The input offset voltage is 75 µV max, and the input noise voltage is typically 0.15 µV p-p from 0.1 to 10 Hz. The MSK-738 hybrid op amp comes in a TO-8 case that provides shielding. Commercial version, $85; military version, $140 (1-24).

M S Kennedy Corp, 8170 Thompson Rd, Clay, NY 13041. Phone (315) 699-9201.

Circle No 352

8-BIT A/D CONVERTER

- *2.5-µsec conversion time*
- *Slew rates to 20V/µsec*



Pin-compatible with the ADC0820 and ADC7820 converters, the LTC1099 A/D converter features an on-chip S/H circuit. The device has a 2.5-µsec conversion time and can handle slew rates to 20V/µsec. All edge-sensitive timing circuitry for the LTC1099 is internal to the device, thus eliminating the need for external pulse-shaping and timing circuits. Its 3-state control permits easy interface to a µP data bus or an I/O port. The LTC1099 provides two modes of operation, Read and Write-Read, and an overflow output for cascading the devices. A Stand-Alone mode permits operation without the use of a µP. The device, which operates from a 5V supply, has analog and reference inputs of −0.3V to V_{CC}+0.3V and a digital input range from −0.3 to 12V. The device comes in a plastic or a ceramic DIP. From $8.25 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545.

Circle No 353

Text continued on pg 249

there IS JUST ONE way to Raise THE Standards in Computer graphics.

Our Bt458 set the standard for workstation color graphics. Now we say "standard" is not enough.

Question authority. Challenge the status quo. And flex your creative muscles.

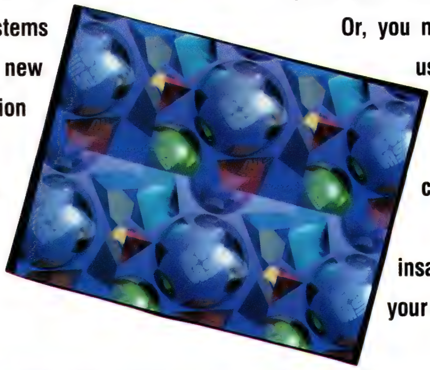
Why? Because it's up to *you* to take computer graphics to the next higher plane.

Which brings us to our legendary Bt458, the industry standard triple 8-bit RAMDAC. For our many customers who have based successful workstation graphics systems on the Bt458, we now offer a plastic package, the new Bt458KPJ with a drastic reduction in power dissipation from the original.

But why be conventional? Go for greatness. Design in the latest wave in RAMDACs instead—our new 135 MHz Bt459.

The Bt459 enables you to stretch the envelope.

A display of brilliance—that's the least we expect from you.



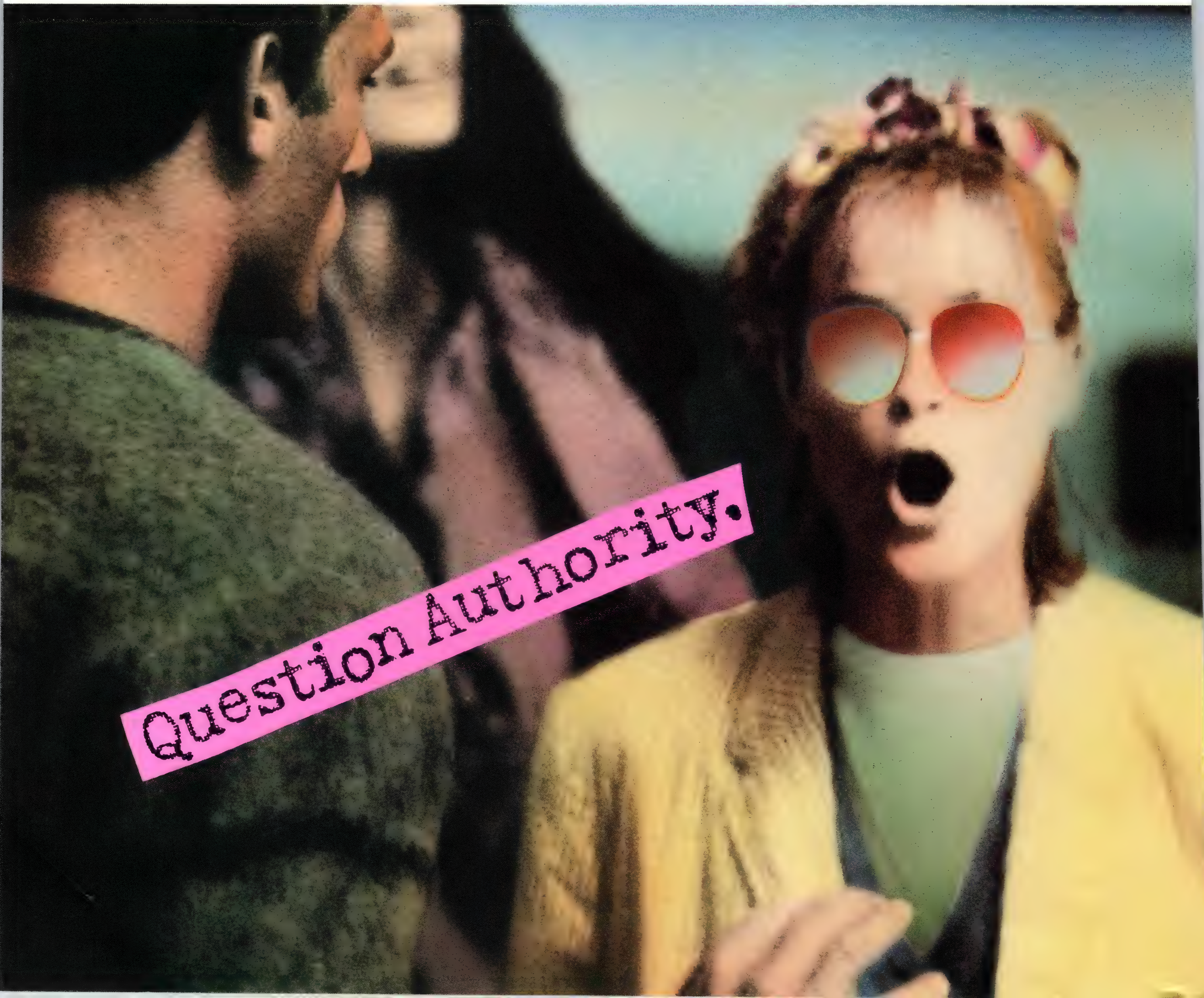
It gives you 256x24 color palette RAM with 16x24 overlay color palette, programmable multiplexing of the pixel and overlay ports, and bit plane masking and blinking.

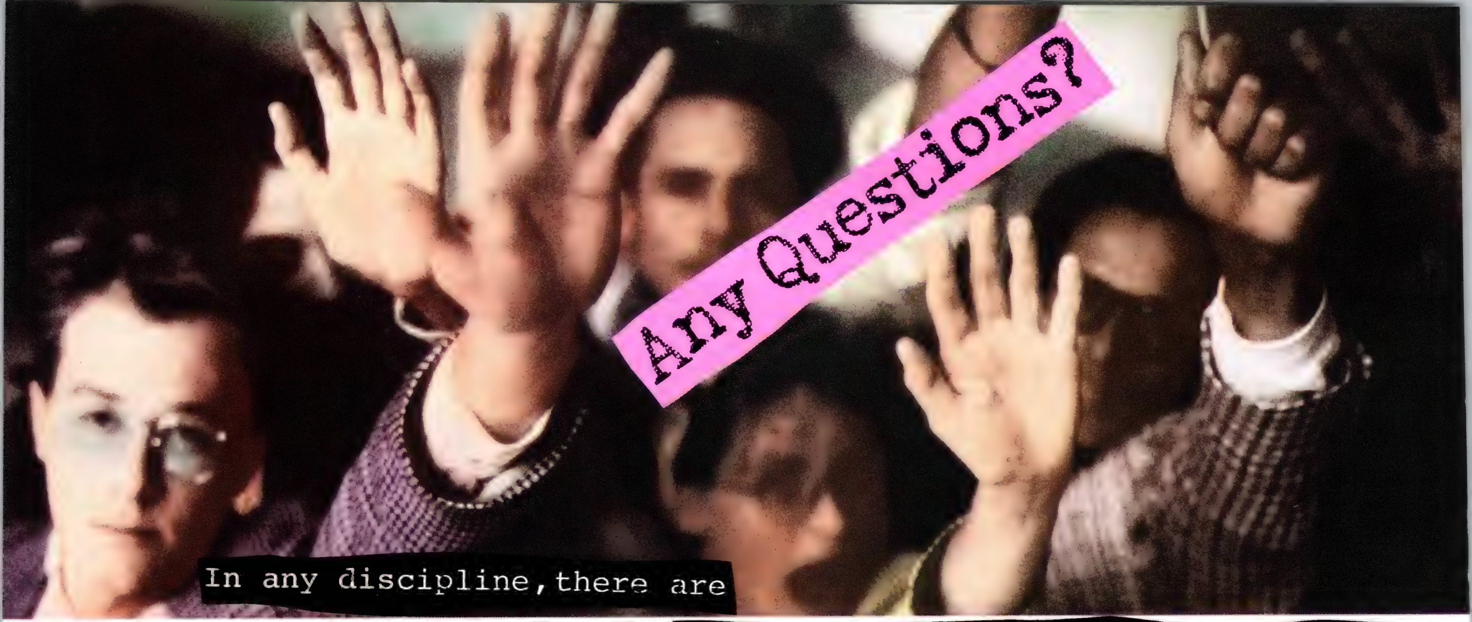
Plus the Bt459 provides 1x to 16x integer zoom support, panning support, cursor control and easy customization of frame buffer dimensions. Imagine the possibilities.

(If all this doesn't get your creative juices pumping, you better move into management.)

Or, you may want to explore true color graphics, using our Bt457 RAMDACs. Unless of course you're of a more radical nature and prefer using 170 MHz Bt461 with five times the color palette.

The point is, if you want to design insanely great workstation graphics, we've got your weapons.





In any discipline, there are followers and there are leaders. Life's more meaningful for the latter.

Q ***Is an 18-bit wide color palette really enough for quality desktop presentation graphics?***

A Why restrict yourself to 256K visible colors when the 24-bit wide Bt473 gives you 16 million colors to work with. It's the smart way to get true 35mm slide quality graphics. Or achieve 24-bit wide pseudo color using the Bt478.

Q ***Anti-aliasing images at a small incremental cost?***

A It's possible. Stick with your 640x480 VGA monitor and use the Bt473. Its anti-aliasing capability provides full true color display without having to upgrade monitors.

Q ***How do you handle D-size monochrome drawings and high-res color graphics in the same system?***

A With the Bt459. Its block mode gives you software selectable virtual resolution. Just unfold the color bit planes—starting at 1280x1024x8—to customize the frame buffer to your application. And since the Bt459 fully supports panning, it enables you to move over an image as large as 5120x2048x1.

Q ***Pan and zoom?***

A Also fully integrated into the Bt459. We use pixel replication techniques to provide cost effective zoom, 1x to 16x.

Q ***How do you cope with multiple applications running simultaneously in a window environment, each requiring its own 256 word color palette?***

A The Bt461 does windows—up to five of them displayed at a time, each with their own color palette. Or you can have a 1024 word palette for pseudo color graphics with an alternate 256 word gamma-corrected true color palette.

Q ***What's the best way to support cursors?***

A Start with our Bt431 for a single 64x64 user definable cursor, designed to talk to the overlay ports of all our high speed RAMDACs. Or take a more integrated approach with the Bt459's user-definable cursor. It provides you a 64x64x2 bit map to play with. So you can create a 3-color cursor or an X windows 2-color cursor.

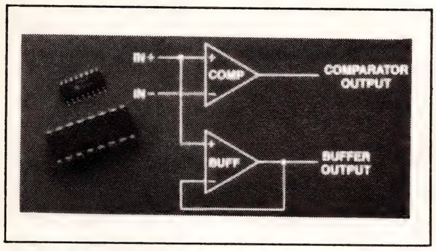
PART	PALETTE SIZE	640 x480	1024 x768	1280 x1024	1600 x1200	APPLICATIONS
Bt450	16x12	✓	✓			Low-end 16-color graphics terminals
Bt451	256x12		✓	✓		Pin compatible, industry standard family for high resolution workstation graphics
Bt457	256x8		✓	✓		
Bt458	256x24		✓	✓		
Bt459	256x24		✓	✓		Next generation workstations
Bt453	256x24	✓	✓			Macintosh compatible
Bt454	16x12		✓	✓	✓	High-end 16-color graphics terminals
Bt461	1280x8		✓	✓	✓	Next generation workstations
Bt471	256x18	✓	✓			Pin compatible family for PS/2 VGA graphics in 44-pin PLCC
Bt476*	256x18	✓	✓			
Bt478	256x24	✓	✓			
Bt473	256x24	✓	✓			True color VGA graphics

* Bt476 also available in 28-pin DIP

Brooktree

Ask us.

We challenge you to be creative. And we provide the fuel to fire your imagination. Nobody offers more RAMDACs, more performance options or functional possibilities. For complete product details on any or all of these products, or if you dare wear one of our "Question Authority" buttons, call Brooktree at 1-800-VIDEO IC. Brooktree Corporation, 9950 Barnes Canyon Rd, San Diego, CA 92121. TLX 383 596



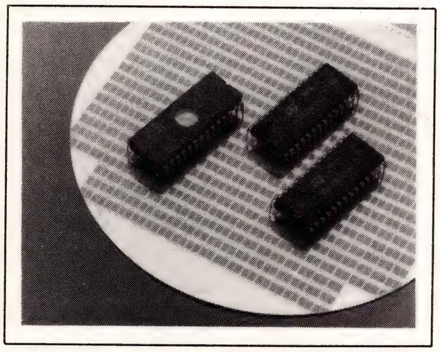
COMPARATOR

- *Low quiescent current*
- *On-chip voltage follower*

Fabricated in CMOS, the MC14578 analog building block contains a low-power comparator and an on-chip voltage follower, which you can use to monitor the noninverting input of the comparator without additional loading. The device operates over a voltage range of 3.5 to 14V, and its quiescent current is only 10 μA at room temperature. Also included on the MC14578 chip are four enhancement-mode MOSFETs that you can externally configure as either open-drain or totem-pole outputs. The comparator needs only a single external component for proper operation—a 3.9-MΩ resistor rated at ±10%. The MC14578 is available in a 16-pin plastic DIP that meets the UL217 specification. $1.34 (500).

Motorola Inc, Technical Info Center, Box 52073, Phoenix, AZ 85072. Phone (512) 928-7944.

Circle No 354



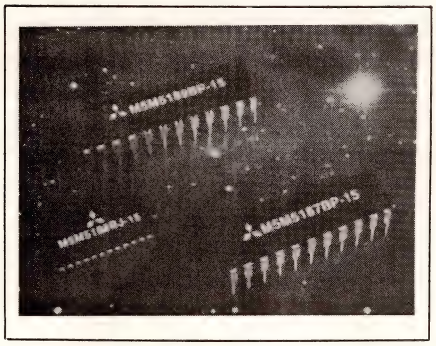
CMOS EPROMs

- *64k and 256k types*
- *Family includes three OTP types*

The 27C256 CMOS UV-EPROM is organized as 32k×8-bits and housed in an industry-standard JEDEC 28-pin ceramic DIP with a quartz window. The programming mode uses a high-speed algorithm, which provides a signature that allows programming equipment to identify the device type automatically. The other three types are one-time programmable (OTP) read-only memories. The 27C64/P and 27C64/FN are 8k×8-bit devices. The 27C64/P version is housed in a 28-pin plastic DIP, and the 27C64/FN version comes in a JEDEC 32-pin PLCC. The 27C256/P is a 32k×8-bit OTP device in a 28-pin DIP. 27C256, $5.25; OTP types, $2.94 to $4.63 (1000).

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100.

Circle No 355



STATIC RAMS

- *15-nsec access time*
- *64k-bit densities*

Combining NMOS memory cells with CMOS peripheral circuitry to create devices with fast access times and low power dissipation, a family of three 64k-bit static RAMs feature access times of 15 nsec. Typical power requirements are 300 mW in the active mode and 5 mW in the standby mode. The 64k×1-bit M5M5187B and the 16k×4-bit M5M5188B are available in a 22-lead plastic DIP or a 24-lead SOJ package. The 16k×4-bit M5M-5189B, which offers an output-enable pin for easier data-bus control, is available in a 24-lead plastic DIP and a 24-lead SOJ package. All devices are available in 15-and 20-nsec versions. From $33 to $42 (100).

Mitsubishi Electronics America Inc, Semiconductor Div, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 356

SMPS CONTROLLER

- *Controls resonant flyback converters*
- *Provides fold-back overload protection and soft starting*

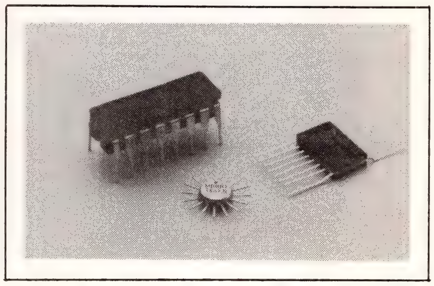
The TDA 4605 switchmode power-supply controller performs all the output regulation and monitoring functions required in free-running flyback converters. Its output provides a direct drive for a MOS power transistor. The controller provides fold-back overload protection, and during output short circuits, it operates in a burst-mode to ensure overload recovery. It also incorporates circuitry to eliminate false switching due to parasitic oscillations in the coupling transformer during short-circuit conditions. Soft-start circuitry limits the inrush current and ensures that the converter's resonant frequency remains outside the audio band as the converter starts up. The controller automatically shuts down the converter if the input voltage falls below a predetermined value. In addition, the device incorporates thermal shutdown circuitry. The TDA 4605 is available in an 8-pin plastic DIP. Approximately $1.50 (10,000).

Siemens AG, Zentralstelle für Information, Postfach 103, 8000 Munich 1, West Germany. Phone (089) 2340. TLX 5210025.

Circle No 357

Siemens Components Inc, 2191 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 980-4500.

Circle No 358



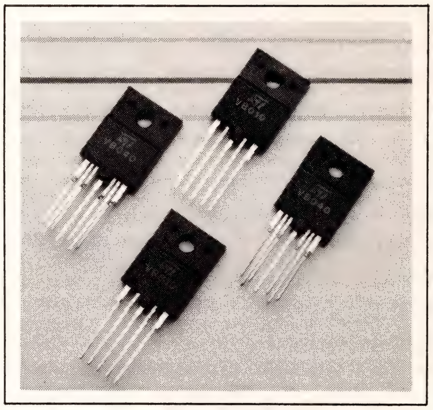
HIGH-SPEED ECL ICs

- *Clock speeds to 3 GHz*
- *Low-power operation*

The MB810 and MB880 ECL circuits are compatible with 10K and 10KH logic levels. Using proprietary bipolar technology, the chips are targeted for high-end test and measurement and telecommunications applications, including fiber-optic transmission. The MB810 series operates at clock rates to 1.5 GHz and consumes from 50 to 150 mW of power. The MB880 series operates at clock rates to 3 GHz and consumes from 250 to 600 mW of power. MB810 devices come in 16-pin ceramic DIPs and 16-pin ceramic axial-lead flat packs. The MB880 series is available in circular ceramic flat packages. MB810, $15; MB880, $120 (1000).

Fujitsu Microelectronics Inc, 3545 N First St, San Jose, CA 95134. Phone (800) 556-1234; in CA, (800) 441-2345.

Circle No 359



POWER SWITCHES

- *Have maximum output ratings of 400V and 7A*
- *Include safe operating area and thermal overload protection*

To improve device reliability, the VB010 and VB040 intelligent power Darlingtons contain output protection and output monitoring circuitry. Both devices have an output voltage rating of 400V and a maximum output current rating of 7A. The short-circuit protection circuitry limits the collector current to 8A, and overvoltage protection automatically turns the output on if the output transistor's emitter-collector voltage exceeds the maximum allowable value. This current- and voltage-monitoring circuitry also ensures that the devices stay within the safe operating area by reducing the collector current as it approaches the boundaries of the safe operating area. Thermal overload protection with a built-in hysteresis of 20°C turns off the output stage if the junction temperature exceeds its maximum value. The device has a TTL/CMOS-compatible control input, and an open-collector diagnostic output that's set to a logic low if any of the device's pro-

tection circuits are activated. The VB040 also has an enable input and separate supply pins for its control and driver circuitry. VB010 $5.30; VB040 $5.50 (100).

SGS-Thomson Microelectronics, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 360

SGS-Thomson Microelectronics, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 361

CMOS EPLD

- *Has four 64-mA quad-state drivers*
- *Has four 48-mA 3-state drivers*

Fabricated in CMOS, the PLX 464 erasable programmable logic device (EPLD) includes four 64-mA quad-state drivers and four 48-mA 3-state drivers. The chip offers direct drive capability of the 60- to 64-mA control signals of the VME Bus, Nubus, Multibus II, and other high-performance buses. The PLX 464 can also drive 8 bits of data to 48-mA drive levels. In addition to the high-current drivers, the PLX 464 includes functions that eliminate the need for transceivers, Schmitt triggers, and other ICs used in bus interface circuits. Other features include bidirectional I/Os, 200 mV of input hysteresis, and two clock inputs. $28.

PLX Technology, 625 Clyde Ave, Mountain View, CA 94043. Phone (415) 960-0448.

Circle No 362

A/D CONVERTERS

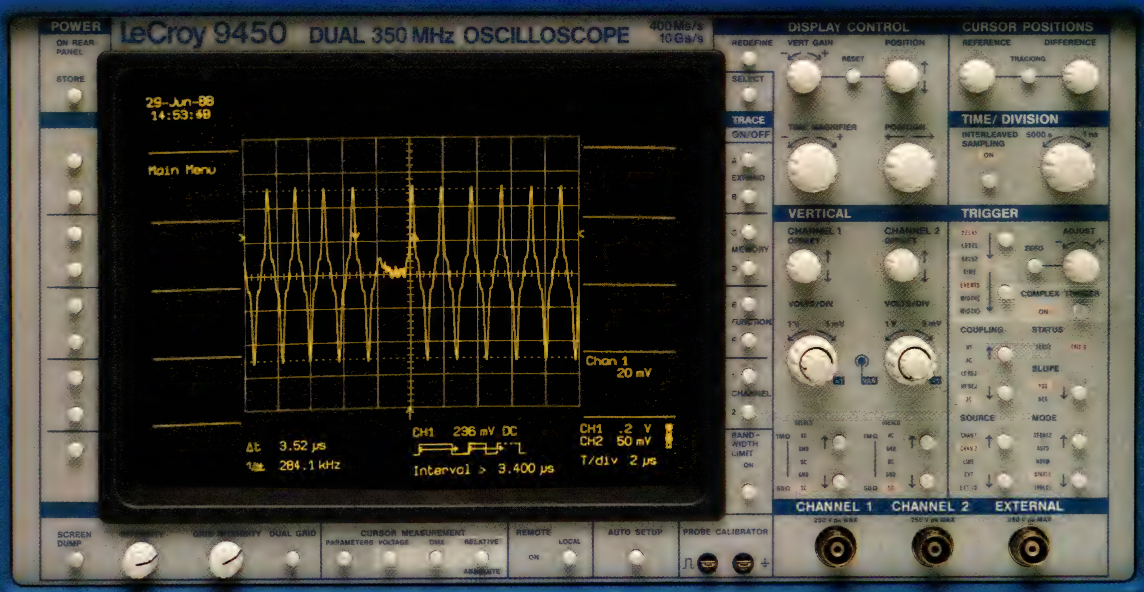
- *12-bit resolution*
- *800-nsec conversion time*

The ADC-520 and ADC-521 12-bit A/D converters have a maximum conversion time of 800 nsec. Both models, which include internal high-impedance buffer amplifiers, are identical except for the analog-input voltage ranges. The ADC-520 has pin-programmable ranges of ±10V, 0 to 10V, 0 to 20V, and 0 to −20V. The ADC-521 has ranges of ±2.5V and 0 to 5V. Performance features include initial errors of only ±3 LSBs max for offset and gain errors, CMOS/TTL compatibility, 3-state outputs, and a maximum power dissipation of 1.9W. Both devices operate from ±15 and 5V dc and are available in either commercial or military temperature grades. Commercial grade, $220; military grade, $242 (1-24).

Datel, 11 Cabot Blvd, Mansfield, MA 02048. Phone (617) 339-3000. TLX 951340.

Circle No 363

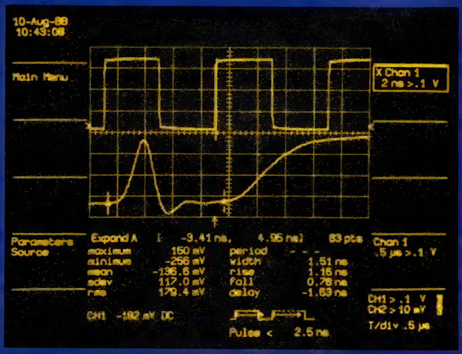
SPEED, FIDELITY and...
...UNPRECEDENTED TRIGGERING



* 350 MHz Bandwidth, 400 Ms/s ADCs
* 50K Non-volatile Memory per Channel
* Glitch, Interval and Logic Trigger Modes
* Automatic Waveform Parameters

NEW! LeCROY'S 9450

THE MOST ADVANCED DIGITAL OSCILLOSCOPE IS DESIGNED FOR YOUR NEEDS.



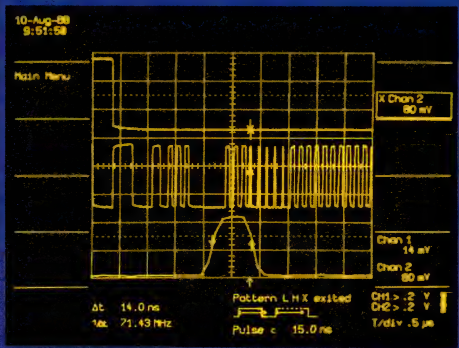
FASTGLITCH trigger mode is used to trigger on a glitch 1.51 nsec wide which occurs before the leading edge of a 500 kHz clock signal (top trace, see trigger arrow at the bottom of the graticule). Fast sampling rates, automatic pulse parameters and horizontal expansion by 250 times (lower trace) all combine to reveal the signal details.

Until now, recording very high-frequency signals with digital oscilloscopes often meant giving up measurement fidelity, due to short acquisition memories, inadequate vertical resolution, or sometimes even both. NOT ANY MORE!!

With LeCroy's new 9450 you get it all, 350 MHz bandwidth, 400 megasample/sec digitizing rates, 8-bit vertical resolution (12-bit with averaging), 50,000 words of acquisition memory per channel and... a uniquely powerful trigger system.

*Glitches, drop-outs, logic patterns and states are all triggered on easily with LeCroy's new and innovative trigger modes. For example, the 9450's **FASTGLITCH** trigger mode can be used to trigger on glitches shorter than 2.5 nsec even when they are buried in complex signals. **INTERVAL** trigger mode can be used to trigger on rare phenomena like missing bits. The 9450's massive memories show more pre- and post-trigger information so you can examine the cause and effect of any signal perturbation. Waveform expansion (up to 1000 times) reveals **ALL** the signal details you are looking for, and fast parameter calculations deliver the answers you need in a fraction of a second.*

*And... you already know how to use it. A familiar front panel, together with a push-button **AUTO SETUP** facility, lets you rapidly learn to operate this new member of the LeCroy oscilloscope family.*



Logic conditions can be individually set for each of the 9450's inputs. PATTERN trigger mode is used to trigger only when the logic condition CH1 Low (top trace) and CH2 High (middle) is exited. The pattern must also be present for less than 15 nsec (lower trace). The trigger position is shown by the arrow at the bottom of the graticule.

To receive further information, technical documentation or a demonstration, circle the reader service card or call us today.

LeCroy Corporate Headquarters
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499
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800-5-LeCroy
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LeCroy

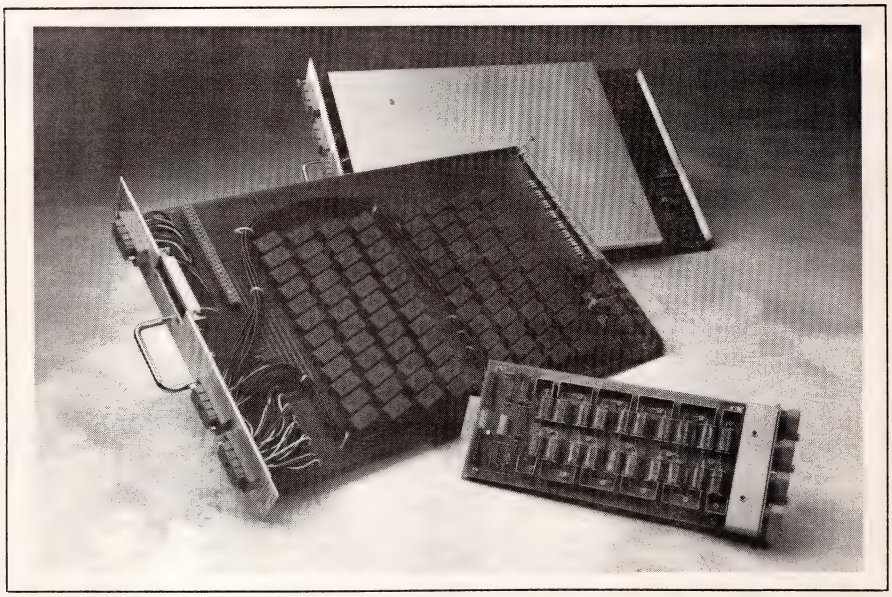
Innovators in Instrumentation

CIRCLE NO 91

TEST & MEASUREMENT INSTRUMENTS

RELAY SCANNERS

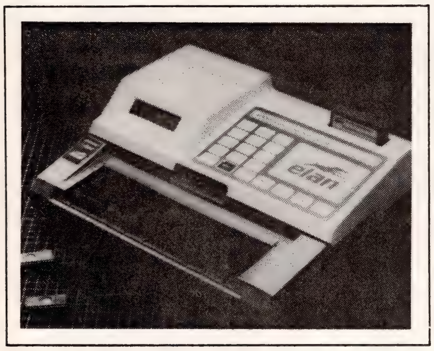
- *Provide configuration flexibility*
- *Switch analog signals for precise measurements*



The 7071-4 and 7074 relay-scanner cards plug into the vendor's 707 mainframe, and the 7152 card plugs into the 705 and 706 mainframes. The 7071-4 contains a pair of 4×12, 3-pole switching matrices that you can connect to make a 4×24 matrix. The 7074 card contains eight 3-pole, 1×12 matrices and is available with dry- or mercury-reed switches. The 707 mainframe accommodates multiple cards and matrices as large as 4×144. The 7152 is a 4×5, 2-pole matrix that you can expand into a 10×4 or a 5×8 matrix. It has an offset current of 1 pA. The 7071-4 and 7074 cards feature a contact potential of <5 μV. Both cards also have a cold-switching contact life of 10^8 closures in dry-reed configurations and considerably more in mercury-reed versions. 7071-4, $2800; 7074 with dry-reed switches, $3200; 7074 with mercury-reed switches, $4900; 7152, $1395.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139. Phone (216) 248-0400. TLX 985469.

Circle No 385



PROGRAMMERS

- *Reduce programming time by 50%*
- *Use extensive diagnostic facilities to ensure high yields*

The 4000 Series includes two models, and the 5000 Series includes five models. The vendor claims that both series program 50% faster than most competitive programmers. For example, an 8-socket unit checks that the device is blank, programs, and verifies eight 512k-bit EPROMs in 52 sec—6½ sec per device. Both series support NMOS and CMOS EPROMs, EEPROMs, and flash EPROMs that range from 32k to 1M bits. The 4000 Series consists of copiers that transfer data from a master device or a host computer into a target device. The 5000 Series allows gang programming as well as programming of sets as wide as 64 bits. From $1995.

Elan Digital Systems, 2162 N Main St, Walnut Creek, CA 94596. Phone (800) 541-3526; in CA, (415) 932-0882. FAX 415-932-1722.

Circle No 386

SCOPE CALIBRATOR

- *Generates voltage- and time-calibration signals*
- *Provides voltages and time intervals in 1-2-5 sequence*

The Model 1400 oscilloscope calibrator provides voltage- and time-calibration signals. The output is a square wave whose amplitude and period you can select. The unit also provides an uncalibrated 1-kHz sine wave. You can set the square-wave amplitude from 1 mV to 100V in a 1-2-5 sequence. Voltage accuracy when driving a 1-MΩ impedance probe is ±0.5%. You can set the square-wave duration from 10 nsec to 0.5 sec, also in a 1-2-5 sequence. The timing accuracy is ±0.015%, and the rise time is <1 nsec. $499.

B&K-Precision, 6740 W Cortland St, Chicago, IL 60635. Phone (312) 889-1448.

Circle No 387

WANT TO TALK SCSI? CALL CIPRICO AT 1-800-SCSI-NOW.

Why talk SCSI with Ciprico? To start with, we're the only vendor with a complete line of high-performance SCSI host bus adapters for Multibus® I, VMEbus, and Multibus II. Each board was designed to optimize performance with its system bus. And consider our experience. Ciprico has over 50,000 boards installed world-wide. Our design expertise provides you with the highest possible performance at the lowest possible price.

But that's not all. Ciprico has *respondability*. We have the largest staff of customer support engineers in the industry to help you resolve any integration problems. Plus software drivers for all major operating systems.

Our SCSI adapters are all based on an 80186 microprocessor, providing a command queuing, pass-through SCSI command software interface. Each board supports SCSI disconnect/reconnect and asynchronous and synchronous transfer rates of 2MB/s and 5MB/s respectively. And a floppy port is optional for cost effective system design.

So if you're currently designing a system based on Multibus I, VMEbus, or Multibus II, give us a call to talk SCSI.

CIPRICO

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CIPRICO LISTENS. AND RESPONDS.

RIMFIRE 3510
SCSI Adapter for VMEbus

RIMFIRE 1500
SCSI Adapter for Multibus® I

RIMFIRE 2500
SCSI Adapter for Multibus® II

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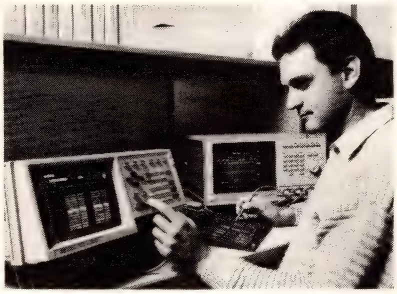
CIRCLE NO 68



DATA GENERATOR

- *Generates pulses and serial data*
- *Operates to 100M bits/sec*

The HP 8118A pulse-pattern generator functions as both a pulse generator and a serial-data generator at data rates as high as 100M bits/sec. The unit, which has 16k bits of memory, has two channels that produce outputs you can vary from 100 mV to 16V p-p into a 50Ω load. A channel-addition mode lets you generate 3- and 4-level signals. When you add channel outputs, you can provide a 32V p-p signal across a high-impedance load. A separate strobe channel operates as a bit, word, or frame trigger. You can independently program timing parameters such as pulse width, transition time, delay, and double-pulse spacing. $12,000. Delivery, six weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 388

DMM OPTION

- *Produces a MATE-compatible systems DMM*
- *Operates in conjunction with self-test and fail-safe options*

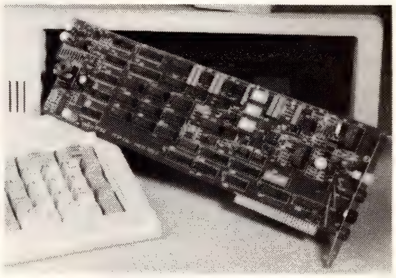
The 70615A option adds MATE (modular automatic test equipment) compatibility to the company's 7061 systems DMM. In addition to providing the DVM with the CIIL (Control Interface Intermediate Language) remote-programming instruction set, the option also implements other systems-oriented features. For example, after a power failure the instrument reinstates the instrument setup that existed before the power failure, and it allows you to capture external events in its 8000-reading nonvolatile memory. If you have the MATE option installed, you can also install the 70616A hardware self-test and 70616B status-monitoring relay options, both of which meet USAF MATE requirements. The self-test option tests the analog functions of the DMM to three test levels, ranging from a simple go/no-go confidence test to full diagnostic checking to board level. The status-monitoring relay option provides fail-safe operation by activating a hardware or system alarm if the DMM's internal μP fails or the instrument overheats. Option 70615A $995; 70616A $395; 70616B $145.

Schlumberger Technologies, Instruments Division, Victoria Rd, Farnborough, Hampshire GU14 7PW, UK. Phone (0252) 544433. TLX 858245. FAX (0252) 543854.

Circle No 389

Schlumberger Technologies, Instruments Division, 20 N Ave, Burlington, MA 01803. Phone (617) 229-4825. TWX 910-250-745. FAX 617-229-4885.

Circle No 390



CALIBRATOR

- *Plugs into IBM PC bus*
- *Produces dc voltage with 4½-digit resolution on three ranges*

The PCIP-Cal is a dc voltage calibrator on an IBM PC bus card. It produces voltages in three ranges with 4½-digit resolution—0 to ±199.99 mV, 0 to ±1.9999V, and 0 to 19.999V. The output, which can supply 25 mA, is short-circuit protected and is isolated from the PC's ground to withstand 500V. The software enables the unit to operate in two modes, which the vendor calls "bench emulation" and programmed. These modes are analogous to the local and remote modes of IEEE-488-based instruments. You program the unit with English-language commands: for example, "SET 15" sets the output to 15V. $895.

Metrabyte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 391

TRANSIENT RECORDER

- *Can store from 512 to 0.75M samples/event*
- *Digitizes to 10 bits at 10M and 20M samples/sec*

The ADA 1000 2- to 12-channel transient waveform recorder allows you to capture, display, and analyze data without additional software. You can perform further data analysis using industry-standard software on an IBM PC or compatible computer. The recorder accepts sampling plug-ins that acquire data at rates as high as 20M samples/sec with 10-bit resolution. Twelve-bit resolution is also available. Programmable-gain, differential-input amplifiers accept full-scale signals from 100 mV to 100V. Each channel can have as many as 64k words of RAM that you can segment or combine to store from 512 to 0.75M samples/event. Depending on the analog resolution, two to six channels of digital storage accompany each analog channel. The unit includes RS-232C, IEEE-488, and matrix-printer outputs as well as multiple analog outputs. $13,275. Delivery, 60 to 90 days ARO.

Soltec Corp, Sol Vista Pk, San Fernando, CA 91340. Phone (800) 423-2344; in CA, (818) 365-0800. TLX 4943094. FAX 818-365-7839.

Circle No 392

CIRCLE NO 63

C COMPILER FOR OS/2

- *Operates with DOS and OS/2*
- *Generates "family-mode" programs compatible with both OSs*

Substantial enhancements in Lattice C Version 3.30 allow it to run under DOS or OS/2. The package's API (Applications Programming Interface) library and Bind utility let you develop programs that are compatible with both DOS and OS/2—hence, the term "family-mode" programs. You don't need to purchase an OS/2 programmer's toolkit in order to create such programs. The compiler automatically detects whether it is running under DOS or OS/2. In the default mode, the compiler generates the correct code for the current OS; however, a command-line switch lets you override the default and select the code generation for DOS, OS/2, or both (family mode). The package also includes bimodal versions of the vendor's screen editor and C-Sprite debugger. You can compile your code from within the editor, and an error-tracking feature displays compiler error messages and highlights the offending lines of source code for immediate correction. $450; upgrade from earlier versions, $75.

Lattice Inc, 2500 S Highland Ave, Lombard, IL 60148. Phone (312) 916-1600.

Circle No 395

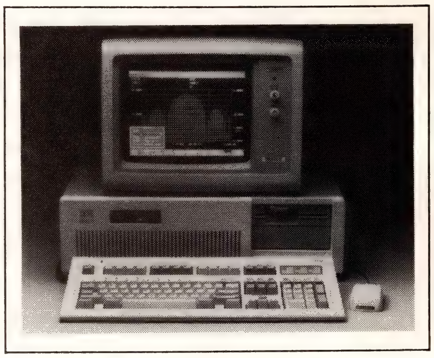
PC MATH LIBRARY

- *Provides ready-to-link libraries for PCs*
- *All routines written in Fortran*

The PC Scientific Fortran Mathematical Subroutine Library Series is organized into several packages that contain ready-to-link subroutines for IBM PCs, PS/2s, and compatibles. You don't need expert mathematical or computer skills to use them; each package includes interactive tutorials that explain all aspects of the routines. All the algorithms have been tested extensively on real-world problems at many mainframe sites. The Minpack1-Lib package solves systems of nonlinear equations and nonlinear least-squares problems. The routines solve the algebra, calculus, and trigonometry problems that arise in scientific and engineering work. The Fitlib routines are based on tension splines and allow you to fit a curve or a surface through any set of points; these routines are particularly valuable in heat-transfer studies, wind-tunnel or turbine design, and fluid-flow analysis. Minpack1-Lib, $465; Fitlib, $695.

McGraw-Hill Book Co, 11 W 19th St, New York, NY 10011. Phone (212) 337-5945.

Circle No 396



MICROWAVE SIMULATOR

- *Can simulate systems with more than 350 components*
- *Files compatible with vendor's other products for integrated design approach*

OmniSys microwave system simulator can model radios, radars, EW (electronic warfare) strips, and feedback control loops. It allows you to observe system response to swept frequency, swept power, multitone spectra, multitone intermodulation, noise parameters, mixer spurious intermodulation, link parameters, and linear control loops. The simulator includes simulations of all mismatch effects. You can perform system tuning and optimization on many output parameter options. The software bases simulations on knowledge of linear and nonlinear system-component data, which can range from simple scalar data to complex component characterizations supplied from external files or generated from inter-

nal models and signal generators. OmniSys runs on IBM PCs and compatibles under MS-DOS or OS/2, Apollo, HP 9000 Series 300, Sun, and DEC VAX. From $12,000.

EEsof Inc, 5795 Lindero Canyon Rd, Westlake Village, CA 91362. Phone (818) 991-7530. FAX 818-991-7109. TLX 384809.

Circle No 397

PARALLEL LISP

- *Operates on Intel Hypercube systems*
- *Runs on as many as 128 80386-based nodes*

This version of Lucid Common Lisp runs on iPSC/2 parallel computers, which are configured with as many as 128 80386-based nodes. You can also obtain hybrid systems with a mixture of nodes that run Lisp and nodes that have an Intel 80387 or a Weitek 1167 vector arithmetic accelerator. Each node may have as many as 16M bytes of memory, which makes the system suited to memory-hungry AI applications. From $15,000 to $30,000, depending on system configuration.

Intel Scientific Computers, 15201 NW Greenbrier Parkway, Beaverton, OR 97006. Phone (503) 629-7629.

Circle No 398

MAC RF

- *Component models include stray and parasitic effects*
- *Provides for frequency-dependent resistors*

RFDesigner is a small-signal analog circuit analysis and optimization tool for RF circuits. The software allows you to perform full nodal analysis and offers random and gradient optimizers, s-parameter libraries, a built-in editor, interactive circuit file creation, automatic error checking of input data files, stability analysis for active circuits, and s-parameter interpolation. You can enter the data through an interactive, menu-driven process that eliminates the syntax errors of other input formats. The graphics output shows you either the input or output parameters in a rectangular or Smith Chart plot with an option for multiple plots on the same axis. The vendor admits that RFDesigner runs more slowly on a MAC II than comparable software running on low-end workstations, but claims that RFDesigner is faster in going from project launching through data-input file creation to hardcopy text and graphics output. You can configure RFDesigner to run on a 1M byte MAC Plus without a hard disk. Because the program currently lacks modeling for waveguides, stripline discontinuities, and noise characteristics, you can't use RFDesigner for microwave design. $1000.

JAG Electronics, 213 Dunview Ave, Willowdale, Ontario, M2N 4H9, Canada. Phone (416) 730-9611. FAX 416-733-3884.

Circle No 399

MULTITASKING TOOL

- *Provides priority or round-robin scheduling*
- *Runs on IBM PCs and compatibles*

Zip is a software component that you use as a building block in creating a real-time multitasking environment. Written in 8086 assembly language and requiring 15k bytes of memory, Zip becomes an extension of MS-DOS and gives control to the command processor as its first task. Zip allows you to make message-passing and synchronization calls. You can also install and monitor hardware interrupts automatically, using Zip's comprehensive interrupt management facility. $995.

Binary Techniques Inc, 35 Medford Street, Somerville, MA 02143. Phone (617) 628-7200.

Circle No 400

EDN PRODUCT MART

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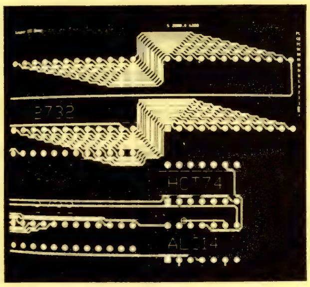
Please circle Reader Service number for additional information from manufacturers.



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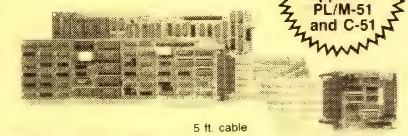

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8051

See EEM 88/89 Page D-1304

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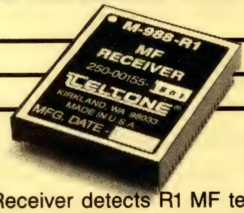

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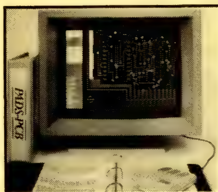

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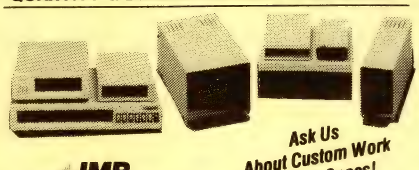

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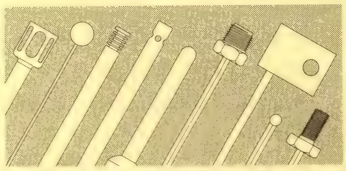

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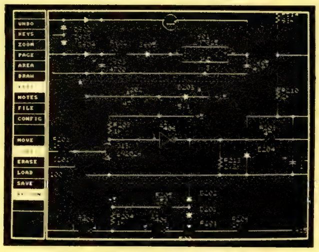

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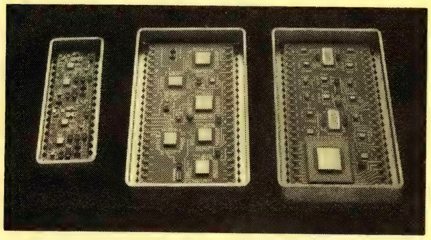

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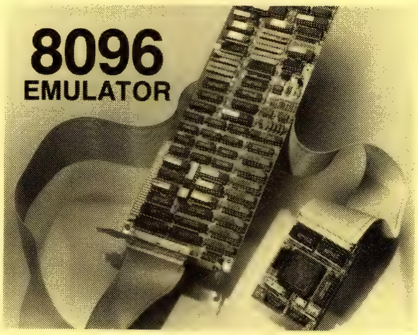

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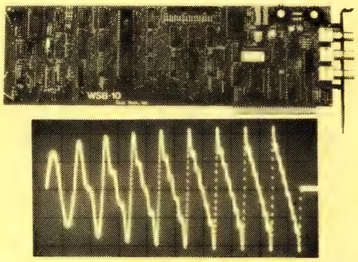

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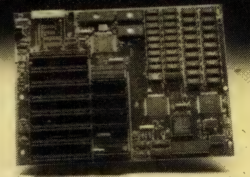

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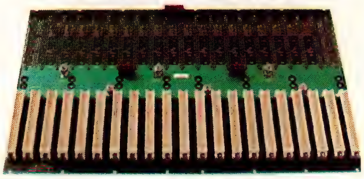

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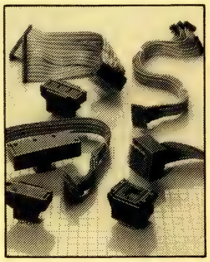

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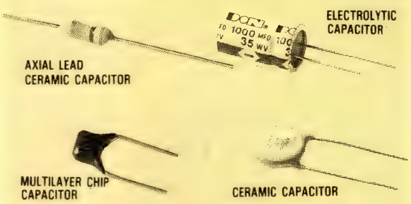

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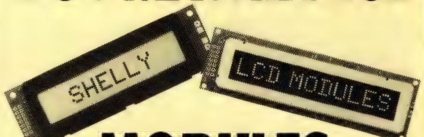

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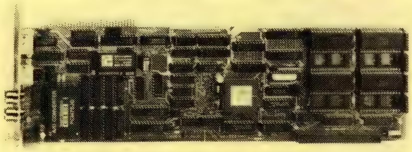

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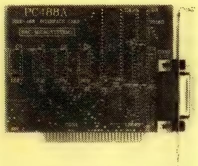

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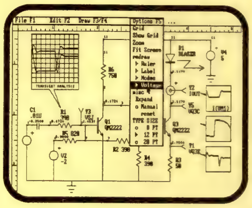

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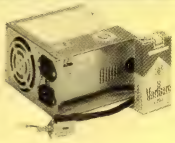

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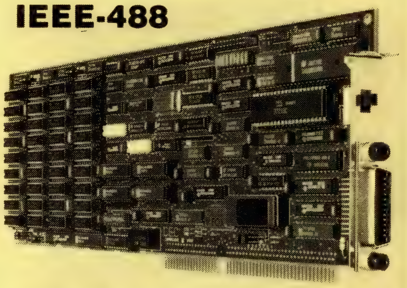

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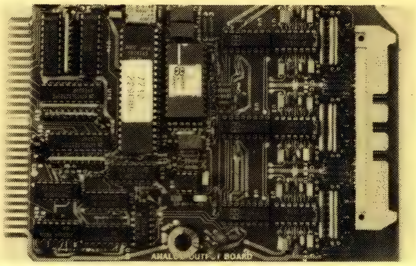

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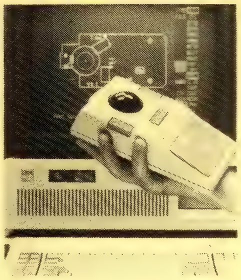

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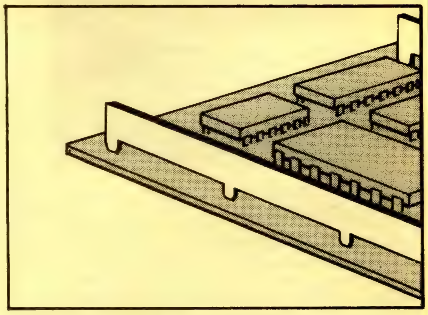

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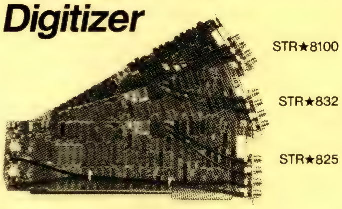

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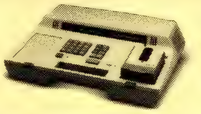

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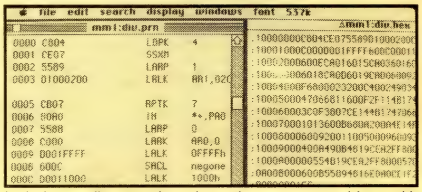

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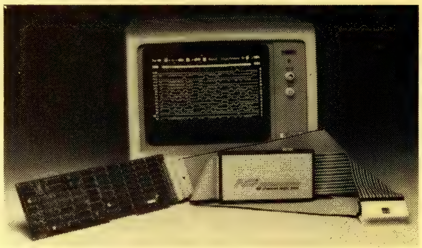

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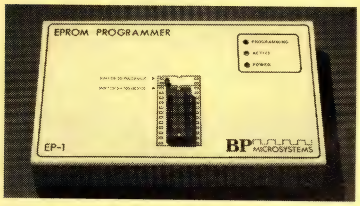

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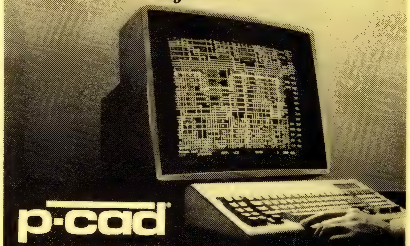

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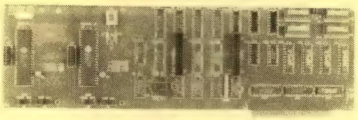

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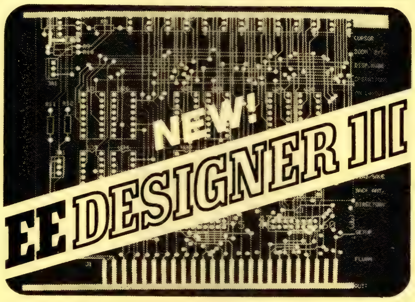

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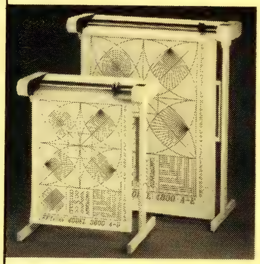

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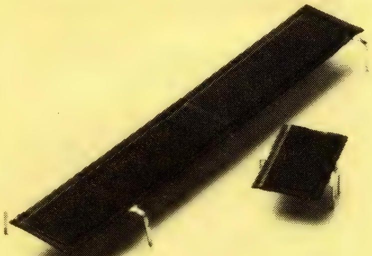

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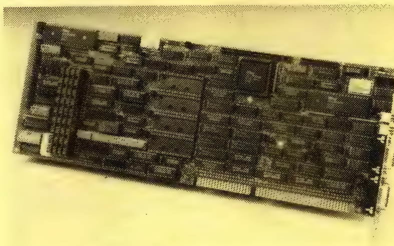

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6809
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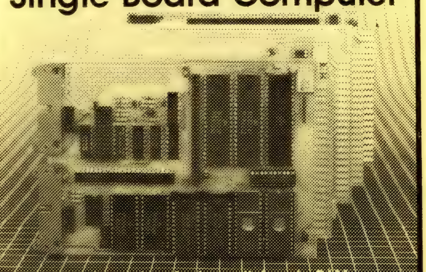

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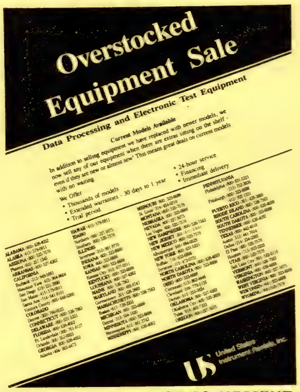

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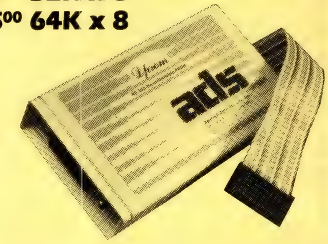

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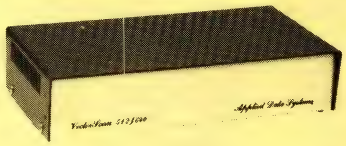

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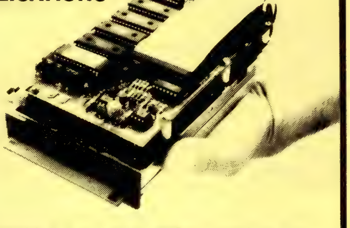

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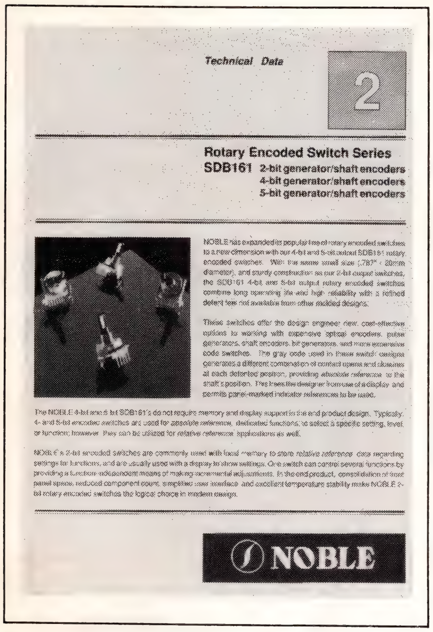


Bulletin covers switches

The vendor's 4-pg technical data bulletin presents the benefits of its SDB161 rotary-encoded switch series. The document claims that the series gives equipment designers an alternative to traditional rotary selector switches, potentiometers used with ADCs, and up/down momentary switches. Mechanical drawings depict dimensional data, and a photograph, specifications, and output-code charts complete the publication.

Noble USA Inc, 5450 Meadowbrook Industrial Ct, Rolling Meadows, IL 60008.

Circle No 430

Product note introduces digital multimeter

The vendor's 16-pg product note explains how the HP 3458A digital multimeter performs high-resolution digitizing. The publication discusses data capture, high-speed data transfers, and waveform analysis software. It also presents an overview of measurement errors that can occur when digitizing waveforms and how the instrument reduces these errors.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 431

Reference for MIL-STD-1750A

This document explains the fundamentals of MIL-STD-1750A. It serves as a reference guide for avionics/aerospace engineers and helps them identify the purpose and scope of the standard. The complete package includes technical data sheets and brochures on MIL-STD-1750A development tools, as well as listings of hardware, software, equipment, and related services.

Sabtech Industries, 3910-B Prospect Ave, Yorba Linda, CA 92686.

Circle No 432

Handbook helps EEPLD users

The 54-pg *Erasic Multi-Level E²PLD TTL Macro Library Handbook* tells you how to implement more than 100 standard 7400 Series TTL building blocks in an EEPLD design, using simple macros. The publication proceeds step by step through the fundamentals of installing the TTL Macro Library and shows you how to implement macros in EEPLD design. It also describes the internal make-up of the macro library and how to use its logic-reduction capabilities. Some of the TTL parts described in the handbook include SSI gates, AND-OR inverters, decoders, multiplexers, comparators, and flip-flops.

Exel Microelectronics Inc, Box 49007, San Jose, CA 95161.

Circle No 433

Brochure sums up STD BusMaster systems

The 6-pg brochure, *The STD BusMaster Series of Industrial Computers,* details the features and applications of the systems and explains how to implement the 80386, 80286, and 8088 processors that are available for them. The publication also includes information about software development. Specifications, diagrams, photographs, and ordering information complete the brochure's content.

Computer Dynamics, 107 S Main St, Greer, SC 29651.

Circle No 434

Summary of microwave laminates

This 2-pg data sheet describes Ultralam 2000 Series woven PTFE microwave laminates. The document presents detailed electrical and mechanical properties of the product and informs you about cladding options.

Rogers Corp, Microwave Materials Div, 100 S Roosevelt Ave, Chandler, AZ 85226.

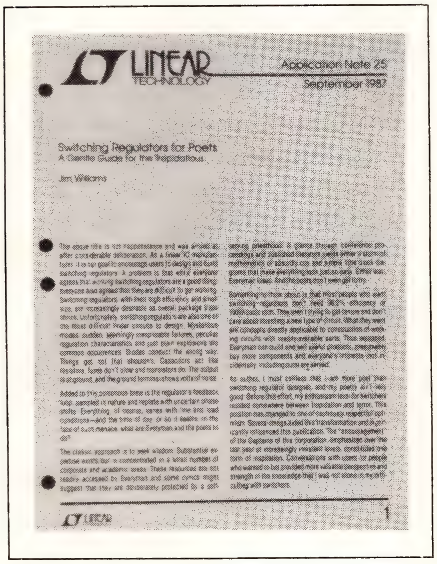
Circle No 435

VXI Bus development-tool packet

This literature packet contains one brochure and four data sheets that describe VXI Bus development tools: the HP E1400A VXI Bus mainframe; VXI Bus development software; the VXI Bus slot 0/translator module; the VXI Bus A/B-size module carrier and the VXI Bus stainless-steel chassis shield; and the VXI Bus C-size register-based breadboard module. In addition to the product descriptions, each document provides specifications and illustrations. The entire packet is 3-hole punched for insertion in a 3-ring notebook.

Hewlett-Packard, 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 436


LINEAR TECHNOLOGY
Application Note 25
September 1987

Switching Regulators for Poets
A Gentle Guide for the Trepidatious

Jim Williams

Take note of switching regulators for poets

The application note, *AN-25: Switching Regulators for Poets*, describes a basic flyback regulator, a −48 to +5V telecomm flyback regulator, a fully isolated telecomm flyback regulator, a 100W off-line regulator, a switch-controlled motor speed controller, and a switch-controlled Peltier 0°C reference. The 24-pg publication includes complete schematics and component values of test circuits. It includes discussions on switching-regulator ICs and frequency compensation of the devices; it also provides a checklist for switching-regulator design and advice on how to evolve a design.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

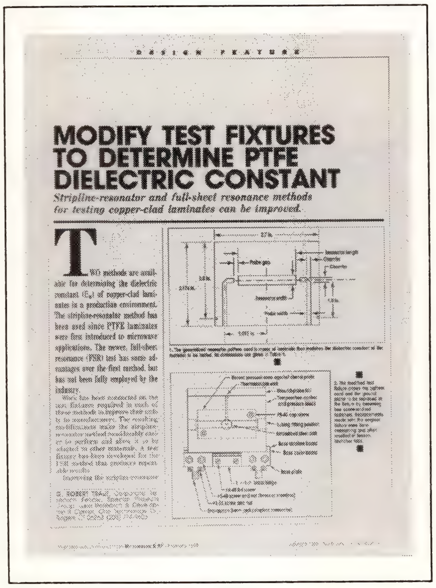
Circle No 437

Articles present phase-locked loops

Document #AR254, a series of articles that discusses phase-locked-loop design, provides detailed information from four separate, previously published articles. The first two articles explain how to analyze and optimize type-2, third-order PLL systems and provide calculator programs for the HP 25 to perform the computations. The third article shows how to suppress sidebands. The final article demonstrates how to calculate the noise spectral density and short-term frequency stability in a PLL with a programmable calculator and vary the parameters to trade off noise/functional performance requirements.

Motorola Inc, Literature Distribution Center, Box 20912, Phoenix, AZ 85036.

Circle No 438


DESIGN FEATURE

MODIFY TEST FIXTURES TO DETERMINE PTFE DIELECTRIC CONSTANT

Stripline-resonator and full-sheet resonance methods for testing copper-clad laminates can be improved.

Article presents PTFE-based laminates

The 4-pg reprint, *Modify test fixtures to determine PTFE dielectric constant,* reports on two methods for finding the dielectric constant of PTFE-based microwave laminates: the traditional stripline-resonator method and the full-sheet resonance (FSR) method. The article comments on the improvements in the test fixtures used for stripline-resonator testing. The resulting modifications have made this method easier to use in a manufacturing environment. The paper also describes a fixture for FSR testing that produces repeatable results and notes that FSR testing is nondestructive.

Rogers Corp, Box 700, Chandler, AZ 85244.

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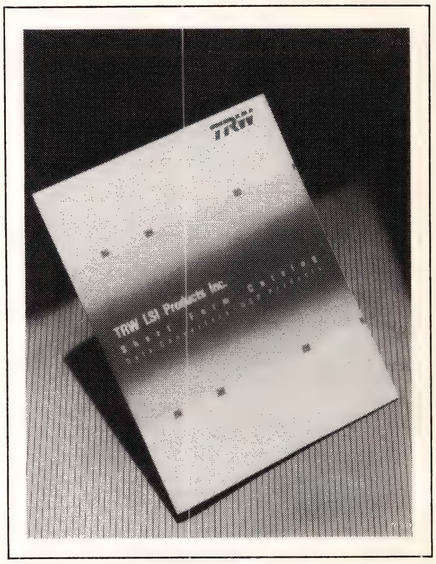

Booklet highlights ICs and hybrid circuits

The vendor's 12-pg catalog includes new data about its integrated circuits, hybrid circuits, and board products. Among these are ICs for data acquisition and digital signal processing. In addition to an overview of the vendor's LSI devices, product sections in the updated publication include ADCs, DACs, advanced arithmetic products, imaging products, multipliers, multiplier/accumulators, memory/storage products, correlators, and packaging.

TRW LSI Products Inc, Box 2472, La Jolla, CA 92038.

Circle No 440

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1988 Editorial Calendar and Planning Guide

EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	Mailing: Dec. 15

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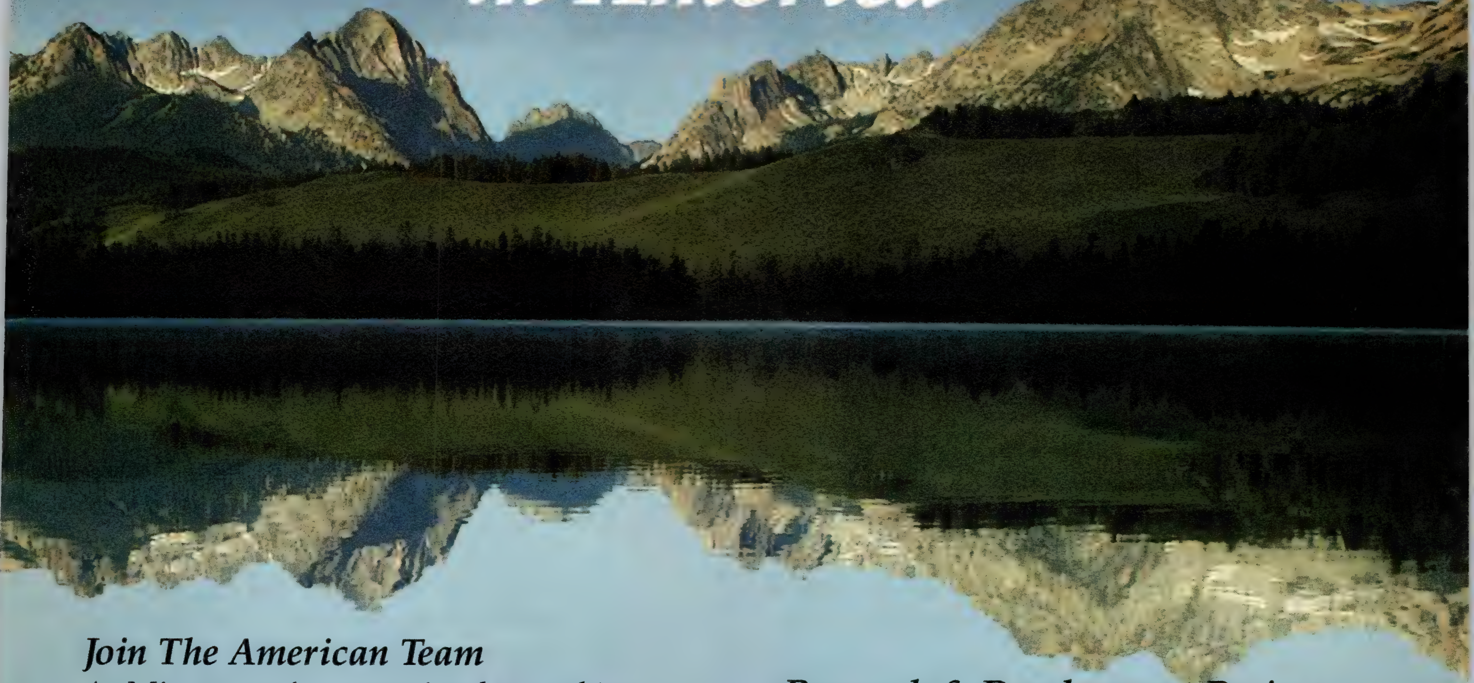

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☐ WILL RELOCATE ☐ WILL NOT RELOCATE ☐ OTHER ______

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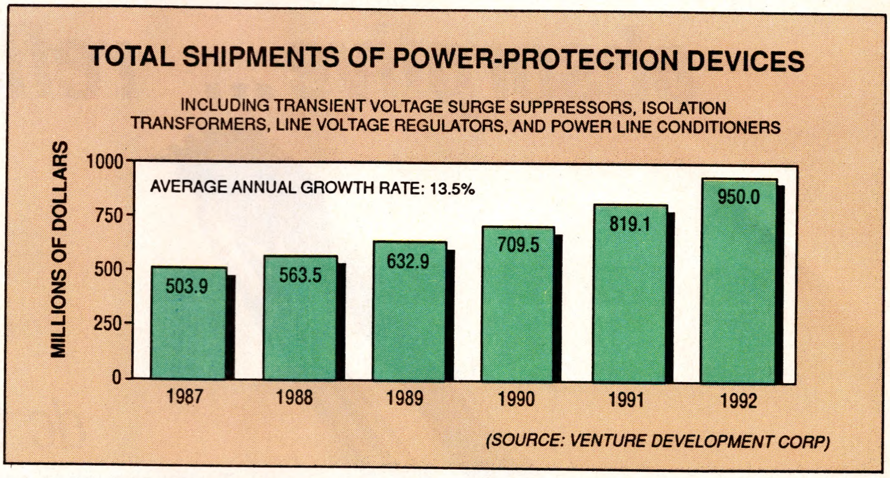
Electric-power demand fuels protection-device market

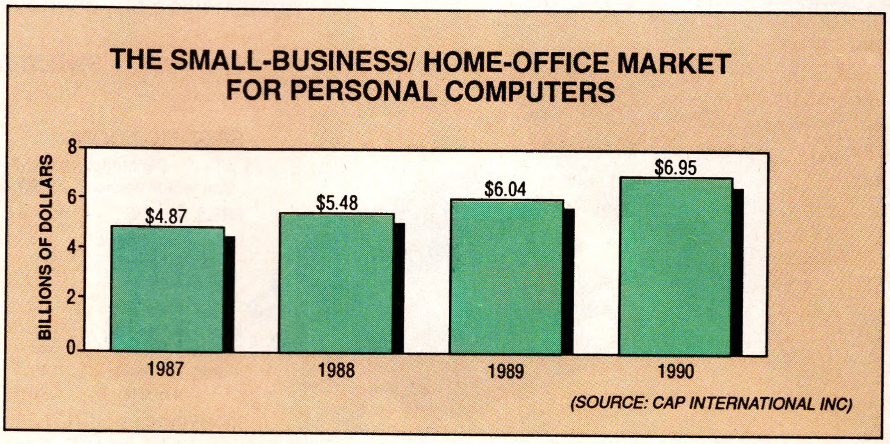


The need for more and more electric power in densely populated areas in the US and the need to protect systems in areas subject to extreme weather conditions are two of the factors that are driving a healthy power-protection market. Power-line disturbances resulting from network switching by utility companies and from lightning strikes to power grids can damage or totally prevent systems from operating. The demand for products to protect electrical/electronic systems and equipment from transient voltage surges, electrical noise and voltage surges, sags, and brownouts will result in a $950 million market in 1992, forecasts Venture Development Corp, a market-research company based in Natick, MA.

Totaling almost $504 million last year, the market for power-protection devices, which includes transient voltage surge suppressors, isolation transformers, line voltage regulators, and power line conditioners, will experience an average annual growth rate of more than 13% in the 1987 to 1992 forecast period. Although shipments of isolation transformers and power line conditioners will increase during this time frame, it will be transient voltage surge suppressors that will lead the pack. Shipments of those products will increase at more than twice the rate of shipments of isolation transformers and power line conditioners.

Behind this trend is a polarization of the US market for power-protection devices, according to Venture Development. The company believes that users are buying transient voltage surge suppressors because they are the easiest and least expensive solution to power problems. And in applications areas where uninterruptible power supplies are not suitable or cost effective, users are going with isolation transformers, line voltage regulators, and power line conditioners.

More PCs going into home offices and small businesses



Sales of personal computers to home offices and small businesses show no downward trend. The market for these personal computers, which totaled approximately $4.8 billion in 1987, will show another large increase in sales during the next two years, according to CAP International Inc. The Natick, MA, market-research and consulting firm forecasts a $6.04 billion market by the end of next year; in 1990, sales should be close to the $7 billion mark.

With this much at stake, manufacturers and resellers of personal computers are beginning to realize that selling in the home-office/small-business segment will require different marketing strategies. Many companies are familiar with the needs of customers who place large orders and are adept at reaching the big accounts. The new challenge will involve learning how to monitor and deal with the "onesie, twosie" needs of users who place their computers in home and small businesses.

And it's no surprise that IBM has already taken the initiative to grab a good portion of the market. The company has targeted desktop publishing and small business as two rapid growth areas, according to CAP International, and seems ready to ensure that resellers can meet the needs of small businesses and still generate a profit.

tiny SPDT switches

absorptive... reflective

dc to 4.6 GHz from $32.95 (10-24)

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Despite its extremely tiny size, only 0.185 by 0.185 by 0.06 in., these switches provide 50dB isolation (considerably higher than many larger units) and insertion loss of only 1dB. The absorptive model KSWA-2-46 exhibits a typical VSWR of 1.5 in its "OFF" state over the entire frequency range. These surface-mount units can be soldered to pc boards using conventional assembly techniques. The KSW-2-46, priced at only $32.95, and the KSWA-2-46, at $48.95, are the latest examples of components from Mini-Circuits with unbeatable price/performance.

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Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model	**KSW-2-46**		**KSWA-2-46**	
Connector Version	**ZFSW-2-46**		**ZFSWA-2-46**	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (db)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ) ON	1.3:1		1.3	
OFF	—		1.4	
SW. SPEED (nsec) rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm) up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	**$32.95**		**$48.95**	
	$69.95		**$79.95**	

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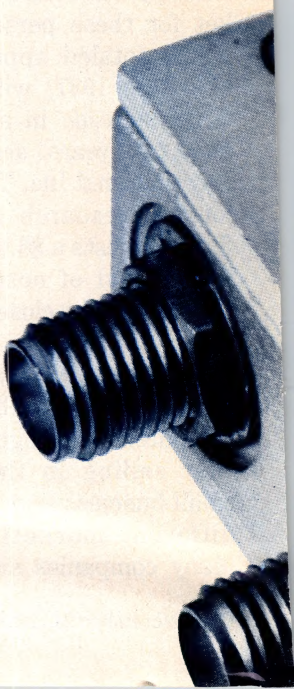

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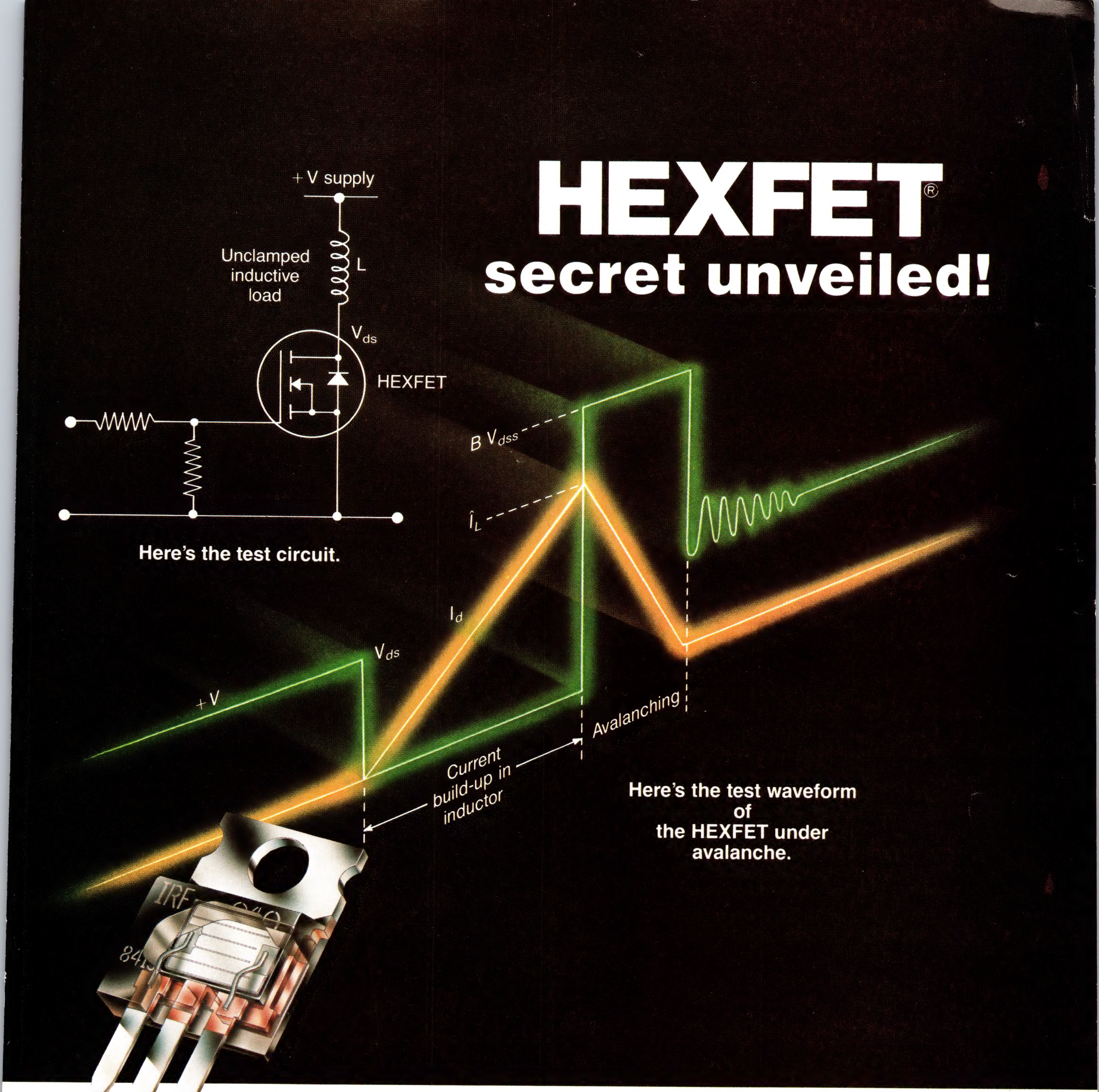

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